

MARCH 1991

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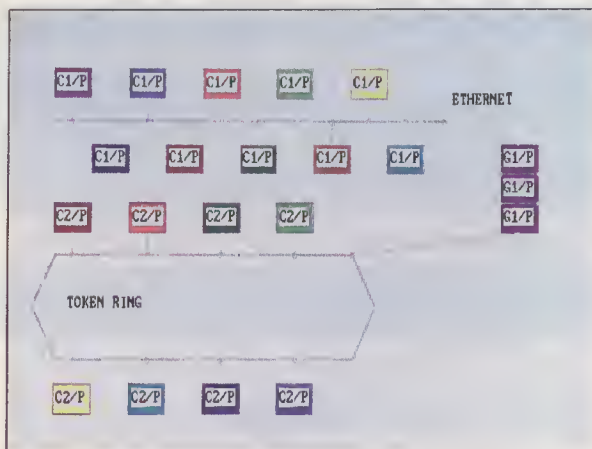


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IEEE COMP

# COMPUTER

March 1991

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## COMPUTER

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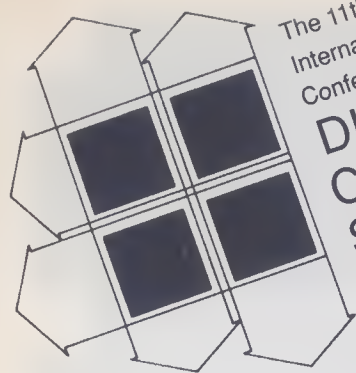
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### HOTEL

The conference will be held at the Arlington Hilton Hotel, 2401 E. Lamar Boulevard, Arlington, TX 76006. Rates for ICDCS-11 are: One person \$66, Two persons \$66, Alcove suite \$85, Penthouse \$225. Hilton reservations phone 1-800-527-9332.

## TUTORIALS

### MAY 20

**Parallel Processing: Architectures and Software**, L. Bic and A. Nicolau, Univ. of California at Irvine  
*Half Day, 9am-12:30pm*

**Parallel Processing: Algorithms and Systems**, H.J. Siegel, Purdue Univ.,  
*Half Day, 1:30pm-5pm*

**Distributed Software Engineering**, S.M. Shatz, Univ. of Illinois at Chicago  
*Full Day, 9am-12:30pm, 1:30pm-5pm*

**Federated Database Systems for Managing Distributed, Heterogeneous, and Autonomous Databases**, A.P. Sheth, Bellcore  
*Full Day, 9am-12:30pm, 1:30pm-5pm*

### MAY 24

**Fault Tolerant Systems: Principles and Examples**, D.K. Pradhan and A.D. Singh, Univ. of Massachusetts at Amherst

*Full Day, 9am-12:30pm, 1:30pm-5pm*

**The Future of Parallel and Distributed Computing—The Next Decade and Beyond**, Stephan F. Lundstrom, PARSA

*Full Day, 9am-12:30pm, 1:30pm-5pm*

**Distributed Operating Systems: Principles, Examples and Experiences**, A. Trippathi, Univ. of Minnesota  
*Full Day, 9am-12:30pm, 1:30pm-5pm*

## THE PROGRAM

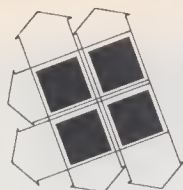
The program will consist of three days of paper presentations and panel discussions (May 21-23) and two days of tutorials (May 20 & 24). More than seventy papers will be presented and three plenary sessions are planned.

## SESSIONS

- Distributed Operating Systems
- Network Performance Models
- Object-Oriented Database Issues
- Distributed Services
- Performance of Parallel Systems
- Object-Oriented Methods
- Distributed Computer System Design
- Probability Models
- Panel on Performance Monitoring for Distributed Systems: Problems & Prospects
- Multicast Communications
- Scheduling in Distributed Systems
- Global Time Issues
- Real-Time Communications
- Load Balancing in Loosely Coupled Environments
- Distributed Mutual Exclusion
- Panel on Protocol Engineering
- Routing & Allocation in Hypercubes
- Concurrency Control and Replications
- Recovery Sets
- Membership Algorithms
- Panel on Distributed Artificial Intelligence
- Multiprocessors
- Techniques for Distributed Algorithms
- Analysis Methods of Distributed Software
- Interconnection Networks
- Fault-Tolerant Distributed Systems
- Distributed Software Applications

## FOR MORE INFORMATION

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| <input type="checkbox"/> Parallel Processing: Architectures and Software <i>Half Day</i>                                              | <input type="checkbox"/> Fault Tolerant Systems: Principles and Examples <i>Full Day</i>                             |
| <input type="checkbox"/> Parallel Processing: Algorithms and Systems <i>Half Day</i>                                                  | <input type="checkbox"/> The Future of Parallel and Distributed Computing—The Next Decade and Beyond <i>Full Day</i> |
| <input type="checkbox"/> Distributed Software Engineering <i>Full Day</i>                                                             | <input type="checkbox"/> Distributed Operating Systems: Principles, Examples and Experiences <i>Full Day</i>         |
| <input type="checkbox"/> Federated Database Systems for Managing Distributed, Heterogeneous, and Autonomous Databases <i>Full Day</i> |                                                                                                                      |

## CONFERENCE AND TUTORIAL REGISTRATION FEES:

Advance Registration - Prior to April 26, 1991

|                            | Member | Non-Member | Student       |
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| Conference only            | \$275  | \$350      | \$45          |
| Tutorials (each, full day) | \$170  | \$215      | \$170/\$215   |
| Tutorials (each, half day) | \$ 85  | \$107.50   | \$85/\$107.50 |

Late/On-Site Registration - After April 26, 1991

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|--|----------|------------|----------------|
|  | \$350    | \$440      | \$45           |
|  | \$215    | \$270      | \$215/\$270    |
|  | \$107.50 | \$135      | \$107.50/\$135 |

Conference registration fee includes admission to the technical sessions, one copy of the conference proceedings, break refreshments and banquet. Student fees do not include banquet. Payment must be enclosed. Please make checks payable to IEEE Computer Society. All payments must be in US dollars, drawn on US banks. Written requests for refunds must be received in the IEEE Computer Society office no later than April 26, 1991. Refunds are subject to a \$50 processing fee. All no-show registrations will be billed in full. Students are required to show current picture ID cards at the time of registration. Registrations after May 3, 1991 will be accepted on-site only.

## AMOUNT DUE:

A. Conference Amount \_\_\_\_\_  
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# LETTERS

## Review challenged

To the Editor:

James L. Johnson concentrates on three issues in his review of my book, *Neural and Concurrent Real-Time Systems: The Sixth Generation* (Computer, Sept. 1990, p. 141). I would like to respond as follows.

(1) Johnson claims that the book is most concerned with networks.

The book covers a much broader topic: design and applications of intelligent real-time systems. Major real-time processes include signal processing, sampling, quantizing, A/D conversion, dead-time losses, mapping, adaptation and learning in neural networks, knowledge chaining, interleaving, concurrency, and reconfiguration. Real-time subsystems include buses, timers, neural chips/cards, and concurrent languages and operating systems. Real-time applications cover sonar, EKG, speech, image, manufacturing inspection, process control, intelligent robots, factory automation, manufacturing, and tomography.

(2) Johnson claims that passages of the book describe product material, excerpted from the manufacturers' literature.

As a rule, real-time systems should be designed from proven manufacturers' modules. Developing proprietary modules requires large investments and produces systems that are incompatible with the rest of the world. The book describes how to design intelligent real-time systems from modules available on the market. In describing the modules, it was necessary to excerpt some data from the manuals.

(3) Johnson claims that the book is qualitative and does not explain underlying principles.

The book explains each underlying principle in minute detail. It describes principles, gives mathematical proofs,

and supports explanations with concrete programs and examples of systems and applications.

It gives special attention to newly discovered principles for system design. These include interleaving of concurrent processes, formation of processor clusters and farms, and reconfiguration of massively parallel computers. The authors of these principles, which represent major breakthroughs in industry, gave permission for their inclusion in my book before their publication in the journals. Based on them, one could design systems with supercomputing power for one tenth the price. For example, the supercluster systems described reached 2,560 MIPS and 386 Mflops (one year later they reached 3,840 MIPS and 575 Mflops).

In conclusion, it is surprising to see a review that carefully avoids the book's subject matter. Thousands of people are using the book as a textbook or reference. They know that it describes *intelligent real-time systems: neural, knowledge-based, and concurrent*.

Branko Soucek

Reviewer's reply:

With respect to point 1, Soucek's list of topics could be properly summarized as a sampling of appropriately chosen signal-processing techniques, leading to certain neural network concepts and their applications. His description then, except for the elaboration of a number of subtopics, agrees with my review.

In point 2, Soucek seems to feel that I take issue with his right to excerpt from the manufacturers' literature. I do not impugn his right to do so. I merely note that the level of enthusiasm for the product is commensurate with the source of the material.

Finally, in point 3, Soucek insists that fundamental concepts are explained in great detail. This is not the case. The very length of the list of design issues he presents argues that a constructive level of detail could not be included in a book of 400 pages. Moreover, Soucek should be informed that the presentation of algorithms in the unstructured Basic language has long since ceased to be good form.

I feel that my assessment of the book is accurate.

James L. Johnson

## Basic software truths

To the Editor:

When Fletcher J. Buckley states the four basic truths about software, he neglects his key truth, "no one uses the design documentation to maintain the code, and no one maintains the design documentation after delivery when the code itself is changed," until the end of the article ("Do Standards cause Software Productivity Problems," *Computer*, Jan. 1991, pp. 97-98). This may be true in many systems, but not in all. Standards are by nature a compromise and may not be applicable to all situations; however, this should not lead us to throw the baby out with the bath water. A better approach might be to tailor the standards to the particular situation at hand.

It may very well be that much of the structure of standards like 2167A originates in the hardware world. However, hardware and software systems are maintained in different ways. Hardware maintenance is focused on component failure. Software is maintained to fix latent errors and to enhance requirements. Consequently, the development and control processes can be expected to be different.

The move to a more structured methodology of software development is aimed at two primary goals. One goal is to introduce good, sound engineering practices in a discipline that very much needs them. The other is to place systems-development controls in the hands of customers.

The target is to provide a better quality software product with reduced life-cycle costs. Based on the lessons learned, we can continue to mold the processes that have become standards and move toward this target.

Robert E. Lane

Author's reply:

The point I was trying to make is that blind, unreasoning adherence to a standard is very costly. The example I used to illustrate that point was the requirement in 2167A for a software physical configuration audit (PCA). I used that example because I know of no one who uses the 2167A documentation (after it has gone through that very expensive process) to maintain or enhance the software. Even worse, I know of no one who is seriously addressing removal of the PCA requirement or looking at the cost-effectiveness of other 2167A requirements. The software problem in the Department of Defense is real, and some of DoD's projected solutions are additional causes of the problem.

Fletcher J. Buckley

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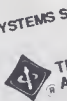
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# CALL FOR PAPERS



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Association for Computing Machinery

The 1991 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN will be held November 10-14, 1991. ICCAD is oriented towards Electrical Engineering CAD professionals, concentrating on CAD for Electronic Circuit Design.

### AREAS OF INTEREST

Original technical papers on (but not limited to) the following topics are invited:

**1) HIGH LEVEL SIMULATION:** Functional, Behavioral, Architectural, Mixed-mode, HDL, Timing Analysis

**2) SIMULATION:** Circuit Timing, Circuit, Device, Process Simulation, Modeling, Manufacturability, Hardware Acceleration

**3) HIGH LEVEL SYNTHESIS:** Functional, Behavioral, Architectural Synthesis, Silicon Compilation, DSP Synthesis, System Design, HDL, Finite-State Machine Synthesis

**4) LOGIC SYNTHESIS:** Combinational, Synchronous, Asynchronous Logic Synthesis, Technology Mapping, Formal Verification, Optimal Clocking

**5) LAYOUT VERIFICATION/ANALOG CIRCUIT DESIGN:** Circuit Extraction/Verification, DRC, ERC, Symbolic Design and Compaction, Cell Layout, Analog Circuit Synthesis

**6) PLACEMENT AND FLOORPLANNING:** Placement, Floorplanning, Partitioning, Area Estimation, Module Generation, Layout Systems, Hardware Acceleration

**7) ROUTING:** Routing for LSI, PCB and Multichip Substrate, Hardware Acceleration

**8) TESTING:** Fault Simulation, Design for Testability, ATPG, BIST, Fault Diagnosis

**9) CAD FRAMEWORKS:** Tool Integration, Design Representation, User Interfaces, DataBases, Design Languages, CASE, Design Management, Total CAD Systems

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Authors should submit:

1) 12 copies of a one-paragraph abstract.

2) 12 copies of the completed paper not to exceed 18 double-spaced pages, figures and tables included.

Excessively long submissions and previously published papers will be returned to the authors.

**NOTE: Papers will be reviewed anonymously.  
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identify authors and their affiliations!**

### FORMAT

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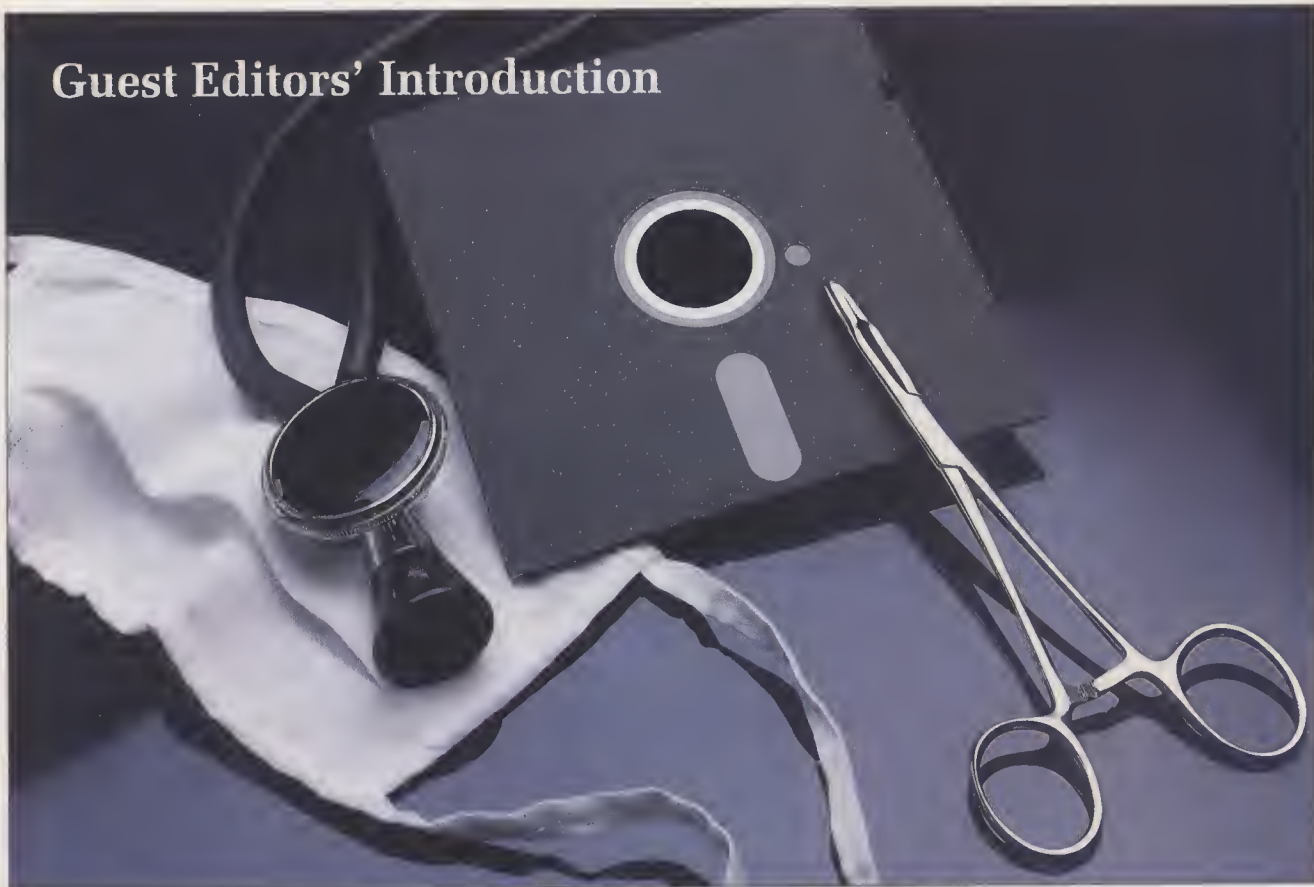
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## Guest Editors' Introduction



# Computer-Based Medical Systems

Timothy J. Kriewall, Sarns 3M

John M. Long, University of Minnesota

**T**o those involved with their development, computer-based medical systems offer unique professional rewards because their application can directly benefit the well-being of mankind.

Imagine for a moment the enormous satisfaction of watching a computer-based heart-lung machine you helped develop sustain the life of a 40-year-old man whose heart is stopped during open-chest surgery. With the machine's aid, the surgical team is extending this individual's productive life. The relationship the perfusionist (the machine's operator) has with the machine is very personal — almost spiritual. Her professional role depends on the machine's

performance, since its function literally means the difference between life or death to the patient.

No one in the operating room thinks about the real-time performance of nine on-board processors and the thousands of lines of C code within the machine — it's simply taken for granted that the machine will work. Yet, millions of dollars and many man-years of effort were applied to making sure the machine would work as the perfusionist, the thoracic surgeon, and, most importantly, the patient require.

Computer-based medical systems fall into two general categories. Like the heart-lung machine, they can be hardware-based systems with embedded computers, or they

can be software-based systems that require advanced PCs or mainframes for their computational or information management power. The first two articles in this issue are examples of the former; the remaining articles deal with the latter.

**Hardware-based systems.** Manufacturers of hardware-based systems face special commercialization challenges compared to the providers of software-based systems.

Today's complex medical device designs can have upwards of 20 processors and 400,000 lines of C++ code to perform functions that discrete component designs performed 10 years ago. Demonstrating

that the system performs as intended is often difficult.

For example, in developing a cochlear implant in which the processor encodes analog voltages to digital stimuli for direct nerve stimulation, no amount of bench testing or animal testing can predict how well a human will hear with this bioelectronic device. The only way to determine the device's success is to surgically implant it. In contrast, complex systems like nuclear therapy machines must be developed with validation as a critical design requirement to prevent unusual operator inputs from creating mega-overdoses to the patient (which has happened).

As Table 1 shows, medical devices can be characterized by function as controllers, information managers, or diagnostic tools. Especially to manufacturers of life-support systems, quality assurance is critical. It is

(Continued on p. 12)

**Table 1. Computer-based medical systems categorized as controllers, information managers, or diagnostic tools.**

| Controllers                | Information Managers  | Diagnostic Tools             |
|----------------------------|-----------------------|------------------------------|
| Fault tolerant:            | Patient records       | Clinical lab equipment       |
| Total artificial hearts    | Network/communication | Blood pressure machines      |
| Heart-lung machines        | Interfaces            | Apnea monitors               |
|                            | Neural networks       | Magnetic resonance imaging   |
| Fail safe:                 |                       | Computerized tomography      |
| Drug infusion              |                       | Positron emission tomography |
| Implantable defibrillators |                       | Ultrasound machines          |
| Nuclear radiation machines |                       | Thermometers                 |
|                            |                       | Audiometers                  |
|                            |                       | EKG machines                 |
|                            |                       | ICU monitors                 |

## For more information

Many applications of computer-based medical systems are not addressed in this issue. The following is an overview of the wide variety of possibilities.

**Clinical assessment and risk evaluation.** Pinette et al.<sup>1</sup> review the use of personal computers in obstetrics, particularly in antepartum and intrapartum evaluation, and address the direction of computer technology in fetal assessment.

Regarding the dilemma of abdominal diagnosis, Paterson-Brown and Vipond<sup>2</sup> describe patient interviews with and without computer-aided diagnostic programs, coupled with various diagnostic means including ultrasonography and laparoscopy. Likewise, Sturman and Perez<sup>3</sup> speculate that the accuracy of microcomputer programs in diagnosing acute abdominal pain can be improved to ultimately outperform the average clinician.

Intravascular ultrasonic imaging of diseased vessels is available in the prevention, diagnosis, and treatment of coronary artery disease. White and Yock<sup>4</sup> describe this field and show how the application of fast Fourier transforms to the Doppler and real-time video spectral displays allows instantaneous modification in positioning catheters within the pulsating coronary arteries to minimize artifacts. In an effort to assess risk, Vatterott et al.<sup>5</sup> describe computerized methods of obtaining and processing signal-averaged electrocar-

diograms to identify those at risk for subsequent ventricular arrhythmias.

Computers are used to increase accuracy, efficiency, and sophistication in evaluating and treating the hearing impaired. Yanz and Siegel<sup>6</sup> review the field and demonstrate how improvement can be made through software changes alone — without the need to purchase more instrumentation.

**Artificial intelligence and expert systems in clinical diagnosis.** With an ever-expanding body of knowledge regarding diagnostic procedures, attempts are being made to employ computers as diagnostic-assistance devices. For example, Beltrame et al.<sup>7</sup> describe the use of artificial intelligence in biomedical image processing. Computer-based expert systems are even applied in the fields of psychiatry (Morelli et al.<sup>8</sup>) and in the treatment of sexual dysfunction (Binik et al.<sup>9</sup>). However, Szolovits and colleagues,<sup>10</sup> who present a complete overview, believe the optimal use of expert systems still escapes developers.

**Medical management.** Therapy is being directly affected by computer-based medical systems. For example, Linkens and Hacisalihzade<sup>11</sup> discuss computer control systems and pharmacological drug administration. Albisser<sup>12</sup> describes



Hospitals and operating rooms are becoming more dependent on computer-based systems for quality health-care delivery. A typical cardiovascular operating room may have a heart-lung machine (lower right corner) containing nine microprocessors to monitor and control life-support processes.

A touch screen on a flat-panel plasma display permits the perfusionist to adjust operating parameters of the machine with the touch of a finger. Attached to the heart-lung machine can be computer-based real-time blood gas monitors (not shown) and database management systems (center left) that automatically make a complete record of the case. These data, in turn, can be coupled to the hospital's health information system through local area networks for cross-referencing by other care providers.

(Photo courtesy of Sarns 3M)

attempts to use microprocessors to manage diabetes mellitus through the use of closed-loop control.

Defibrillation has emerged as the single most effective intervention for resuscitating patients from cardiac arrest. Cummins<sup>13</sup> reviews the electrophysiological basis of defibrillation and ways to increase the effectiveness of counter-shocks, particularly for refractory ventricular fibrillation, which depends entirely on the performance of a microprocessor.

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13. R.O. Cummins, "Defibrillation," *Emerg. Med. Clin. North Am.*, Vol. 6, No. 2, May 1988, pp. 217-240.

equally important to the regulatory agencies charged with assuring product safety.

Regulatory agencies throughout the world are developing new ways to monitor product safety, but few standards exist for medical products with embedded software. In addition to the software within a device, regulatory agencies are concerned with all software involved in making the product, including the production-equipment software and the automated-test-equipment software. It is incumbent on engineers to demonstrate that all software is developed and validated under established practices.

**Software-based systems.** Generally, software-based systems are characterized by their processing ability. They range from health information systems to database managers. Their role is to support knowledge management.

For example, patients are no longer dependent on the knowledge of the local doctor alone. The best medical knowledge is now available to all doctors at their office terminals. Virtually all recent medical knowledge and literature have been automated into Index Medicus by the National Library of Medicine. Artificial intelligence is now required to assimilate the information cataloged in these computer systems. A whole new discipline, variously called medical informatics, medical computing, or computational medicine, is evolving.<sup>1</sup>

Individual patient data are also made more accessible and manageable by computer-based medical systems. Computers are now used in hospitals to track patients, to process and disseminate test results, to assure appropriate medication, to seek in-

surance reimbursement, and to record patient outcomes as a quality-of-care metric.<sup>2</sup> Similar uses are moving into doctors' offices.<sup>3</sup>

**T**he articles in this issue barely sample the recent, exciting advances in computer-based medical systems—the subject is broad and beyond the scope of a single magazine issue. We hope you enjoy the examples we selected. ■

## Acknowledgments

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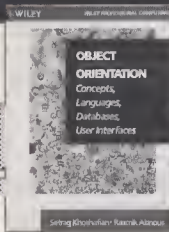
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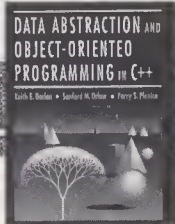
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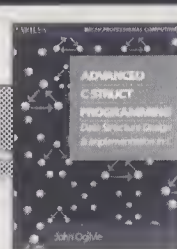
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# Eye Monitor

## Microcomputer-Based Instrument Uses an Internal Model to Track the Eye

Glenn A. Myers, University of Iowa

Keith R. Sherman, Micromasurements

Lawrence Stark, University of California, Berkeley

**A** driver checks the rearview mirror to make sure no cars are approaching from behind, then pulls out to pass the car ahead of him. Just as he pulls out, he sees a large white sedan immediately behind, closing rapidly. He pulls back into his lane and turns around to look for the car he hadn't seen just a moment ago. The "car" was a piece of tissue paper, blown out the window by the wind. It looked enough like a car in size, shape, position, and velocity that the driver actually perceived it as a car.

The common experience of momentarily misperceiving one object as another shows that the human visual system uses internal models or representations of objects during visual search. The shape, color, size, position, direction, and velocity of movement all contribute to the brain's ability to recognize objects quickly.

To track the eye, we use a design philosophy inspired by the human visual system. The eye monitor incorporates an internal representation or model of what the eye looks like to a video camera. The system can measure the position of the eyes and the size of the pupil in the presence of interfering noise, in patients wearing eyeglasses or contact lenses, and in spite of defocus due to small movements in depth by the patient.

### Measurement methods

Eye movements are measured using video techniques, photodiodes,<sup>1</sup> search coils

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**Using an internal model of the eye's geometry, this system makes real-time corrections for head and eye movements while measuring pupillary responses to controlled light stimuli.**

---

embedded in contact lenses,<sup>2</sup> or the optical properties of the eye. Each method has appropriate applications, but we'll discuss only the most widely used methods.<sup>3</sup>

**Video-based systems.** The principal advantages of video-based systems are wide applicability, ease of use with untrained subjects, and the ability to measure the pupil as part of the basic measurement. However, video-based systems cannot resolve eye movements of less than 0.2 degrees or the dynamics of rapid eye movements up to about 100 Hertz. A video-based system developed by coauthor Stark and his colleagues in the 1950s<sup>4</sup> has been de-

veloped further and sold by various companies. Among them are Whitaker, Gulf and Western, and the Applied Sciences Laboratory in Waltham, Massachusetts. This system detects the pupil by finding the transition in brightness of the iris/pupil margin.

We decided to take an approach that is complementary to the edge-detection approach. We detect the lowest frequency object in the image, the contiguous pupil. We have commercialized this system, and it has been sold since 1980 by Micromasurements-Video of Iowa City, Iowa, and by Micromasurements of Farmington, Connecticut.

Another video-based system is offered by I-Scan of Cambridge, Massachusetts. Fairville Medical Optics, of Wilmington, Delaware, offers a portable system<sup>5</sup> for pupil measurement.

**Measuring small, rapid movements.** Other methods are required to measure very small eye movements or to resolve the dynamics of saccadic eye movements, the rapid movements the eye makes as it jumps from one fixation point to another, as in reading, for example.

One measurement technique is to mount pairs of photo transmitters (usually infrared light-emitting diodes) on eyeglass frames, pointing toward the margin between the iris and the sclera (the white portion of the eye) on either side of the pupil. By differentially amplifying the returned light captured by photocells aimed at these margins (more light is returned by

the sclera), it is possible to obtain an accurate measure of gaze angle, with bandwidth exceeding even the fastest saccades. By comparing the movement of the first and fourth Purkinje images (respectively, the specular reflection from the anterior surface of the cornea and the anterior surface of the lens), it is possible to obtain an accurate, high-bandwidth measure of eye position.<sup>6</sup>

Another technique is to embed search coils in contact lenses. Eye movements can then be measured by exposing the coils to two magnetic fields in spatial and temporal quadrature.<sup>7</sup>

## System design

Our eye monitor incorporates an internal model comprising most of what's known about the shape, size, location, and spatial frequency characteristics of the eye's video image. When the eye is viewed obliquely under diffuse infrared illumination, the pupil is elliptical, darker than the surrounding iris muscle, which is fairly bright at IR, and contiguous. Some eye monitors measure pupil size and eye position by detecting transitions in brightness associated with the iris/pupil margin. Such transitions correspond to high spatial-frequency components of the video image. This can be problematic in that high spatial-frequency components are degraded if the patient moves slightly in depth or if corrective lenses intervene. Furthermore, most of the noise in the image (for example, due to eyelashes) is high frequency in content.

**Edge vs. area detection.** If the eye is illuminated along the axis of the camera, light reflecting from the eye's interior results in a bright pupil.<sup>8</sup> Under oblique illumination, as used in our system, the pupil is the darkest object in the camera's field of view. Thus, when the video image of the eye is thresholded appropriately, only the pupil is detected. The pupil area corresponds to the zero spatial-frequency component of the thresholded image. Diameter measurement depends on edge detection, essentially a differentiation process that enhances the sensitivity to high spatial-frequency components in the image. Most of the noise in the image is high frequency in content, whereas the pupil is a contiguous region and hence primarily low frequency in content. Thus, edge detection is sensitive to the noise in the image. Area detection, on the other hand, is sensitive to the low-frequency content of the image,

which improves its signal-to-noise performance.

Measuring pupil area makes physiological sense, since the amount of light on the retina is proportional to pupil area. Area measurement confers signal-to-noise advantages relative to diameter. For diameter measurement, a 1 percent increase in radius results in a 1 percent increase in the measured signal diameter. For area measurement, a 1 percent increase in radius results in a 2.1 percent increase in area. Thus, the signal associated with change in area is twice that due to diameter, resulting in improved signal-to-noise ratio in the presence of additive noise.

The integrative (area) method affords improved resolution. For detection of vertical pupil diameter, resolution is limited by the number of lines in a video frame: 525 in NTSC/RS170 video systems. Each frame comprises two half frames. About 10 percent of the lines are essentially unavailable, since they would occur during vertical flyback. Thus, only about 240 lines of resolution are truly available in each half frame. The video refresh rate is 59.94 half frames per second. For horizontal diameter measurements, resolution is limited by the number of pixels (picture elements) in a scan line. This is about 250 but may vary widely between cameras. The resolution of area measurement systems is limited by the total number of pixels per frame:  $240 \times 250 = 60,000$ . Of these, about half (30,000) could be occupied before the edges of the (circular) pupil fall outside the (rectangular) field of view.

In some applications, we may want to record pupil diameter rather than area. Area is optionally converted to diameter in real time using a lookup table stored in PC RAM. The corrections and conversions described here use lookup tables for speed, since these and several other calculations must be completed in less than one video half frame (16.7 milliseconds).

**Circular tracking window.** Because the edges of the video field tend to be dark, they would ordinarily be detected as part of the pupil. To prevent this, a circular window centered on our estimate (updated every half frame) of the center of the pupil disables the pupil-detection hardware outside the window. This window tracks the eye in real time by computing the distance from the apparent center of the pupil ( $a, b$ ) and enabling the counters when this distance is less than a value set by the operator. This is accomplished by taking the two's complement of the coordinates  $a$

and  $b$  and adding then to the  $x$  and  $y$  values, respectively, of each pixel during the scan. These differences are squared with hardware multipliers, and their sum compared to the  $r^2$  value input by the operator. When the window is initialized or reinitialized following a blink, the nominal position of the center of the pupil is the center of the video frame for initialization or the last valid position following a blink. If a portion of the pupil is within this window, the window centers on that portion, which causes the window to converge on the pupil center.

If pupil size falls outside a physiologically plausible range (3-50 mm<sup>2</sup> in area), the computer recognizes this as a blink, stores the last valid position of the eye for five half frames, and holds its position, waiting for the eye to reopen. If pupil area is still out of range after this interval, for example, if the patient's eye moves during a blink, the eye monitor searches for the eye by increasing window size.

**Measurement errors.** Eye movements can introduce errors in pupil size measurement. If a patient looks straight into the camera, his pupil appears as a circle. If he looks to the side, his pupil image is an ellipse whose major axis is vertical. If he looks up or down, the major axis is horizontal. In either case, there is a compression of the apparent extent of the pupil along the axis of gaze. The minor axis and thus the solid angle of subtense of the pupil viewed by the camera (taken to be at infinite distance, relative to the dimensions of the eye) are multiplied by the cosine of the gaze angle. The eye monitor corrects for this error (to within 1 percent for angles up to 45 degrees) by multiplying apparent pupil area by the secant of the gaze angle.

Head movements are the largest source of errors in eye position measurements. Most often, these comprise small translational movements, which appear on the video as changes in apparent eye position. These result in "corrections" of the types discussed above. To avoid introducing errors of this new type, it is necessary to monitor head position as well as pupil position. The difference between the center of the pupil and that of the first Purkinje image (FPI) is a first-order invariant with respect to translational head movements. The center position of the FPI is subtracted from that of the pupil, yielding a measure of gaze angle corrected for small head movements. As gaze angle increases, the incremental change in the position of the pupil center seen by the camera is reduced

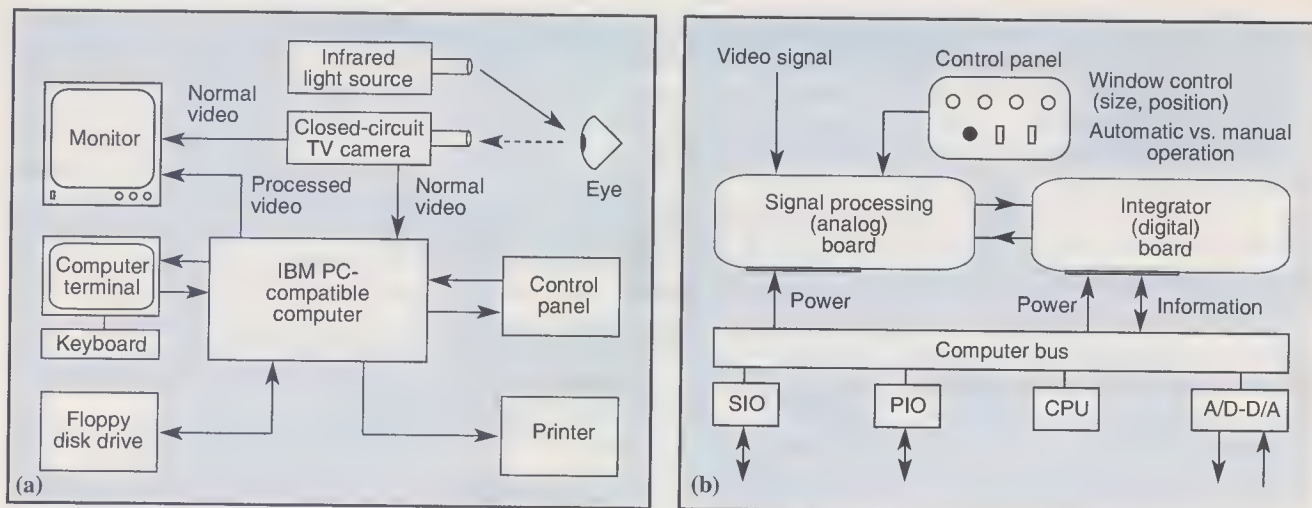


Figure 1. Block diagram of the eye monitor: (a) the components of the eye monitor, including the computer, TV camera, TV monitor, and infrared light source; (b) the eye monitor boards that reside on the PC AT bus. The control panel allows the operator to choose either automatic mode (in which the circular window tracks the eye) or manual mode (in which the window is stationary) and to control the size and (in manual mode) the position of the circular window. The pupil threshold is controlled by the up/down arrows on the keyboard.

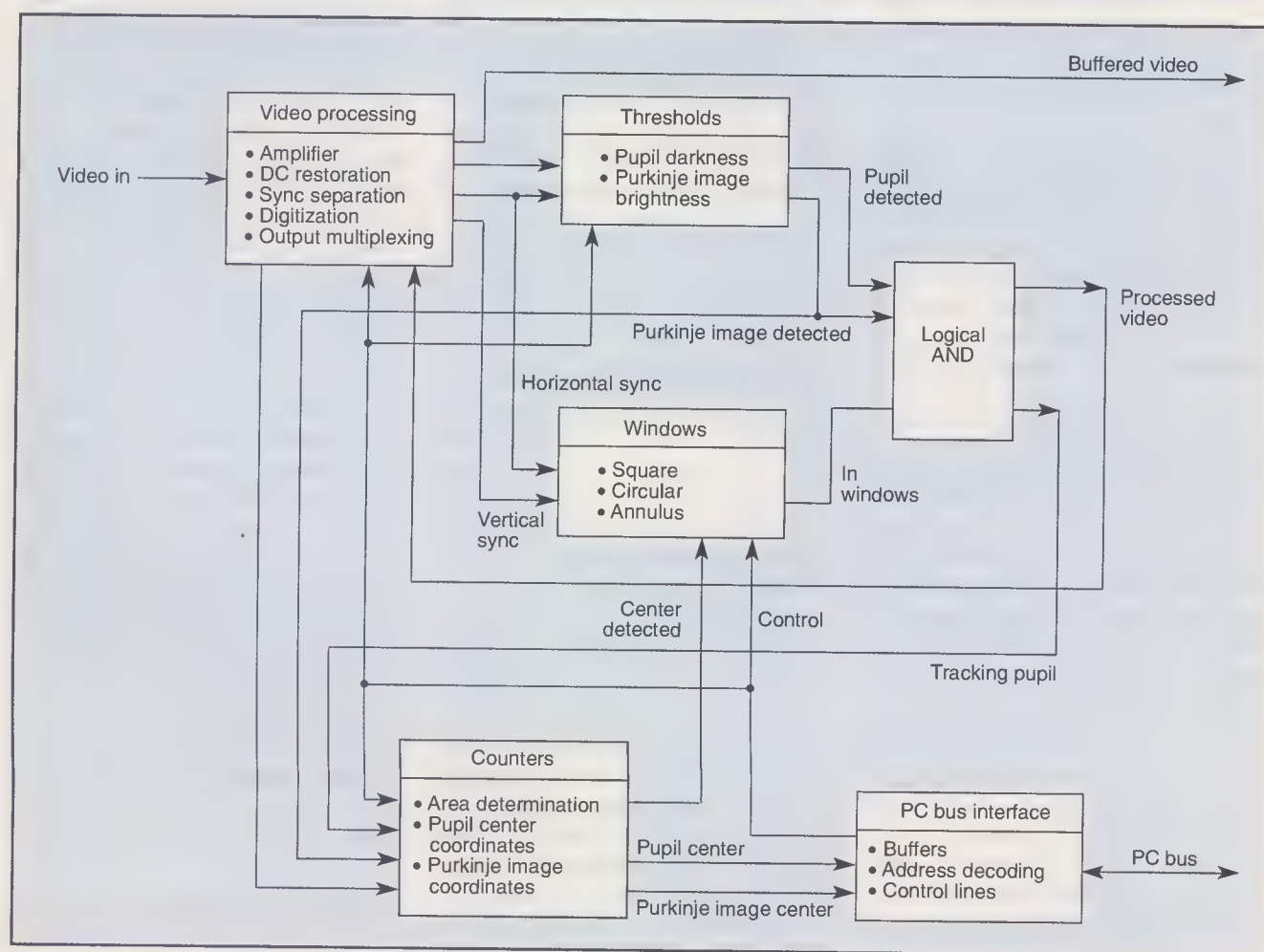


Figure 2. Block diagram of the eye monitor hardware, showing the video processing, thresholding, windowing, and other circuits.

approximately by the cosine of the incremental gaze angle. Apparent gaze angle is corrected by multiplying it (via lookup table) by the integral of the cosine of the gaze angle.

Taken together, the integrative (area) measurement method, circular tracking window, hysteresis, search algorithms, and correction schemes constitute an internal model. That is, the methods used to capture pupil and eye movement signals employ much of our knowledge about these systems. For example, we know that the pupil is a dark, contiguous circular area, so the threshold is set to detect darkness. The hysteresis and the integrative approach both emphasize low spatial frequencies (that is, large contiguous blocks). The window is circular, as is the pupil. The system knows that the physiological range of pupil area is 3 to 50 mm<sup>2</sup> and that the eye usually cannot

move fast enough to leave the window during a blink, so a search algorithm is triggered when pupil size falls outside these values.

## System description

**Hardware.** A charge-coupled device (CCD), black-and-white television camera (Panasonic WV-BL200) captures an image of the eye illuminated by an infrared light source (Figure 1). The video signal from the camera goes to the eye monitor hardware, which resides on two boards on the IBM PC AT bus. The signal is DC restored, amplified, and digitized by a video digitizing chip (Analog Devices AD9502). Horizontal and vertical blanking and synchronization pulses are stripped out and routed for use elsewhere. The vid-

eo signal is compared with a threshold (Figure 2) controlled by the operator from the keyboard. When the video signal is darker than the threshold level, the system interprets this to mean the scan is within the pupil, and a counter (C1) is enabled (Figure 3). The counter is driven by the camera pixel clock. At the end of a video half frame (that is, when the scan reaches the bottom of the screen), the contents of the counter are proportional to the (uncorrected) pupil area. At the end of a half frame (signalled by the vertical refresh pulse), all counters are latched, and the software reads the contents of C1 as pupil area.

To find the center of the eye, this area is divided by two with a hardware shift down one bit, and the contents of another counter (C2) are filled with this half area. In the subsequent half frame, counter C2 is dec-

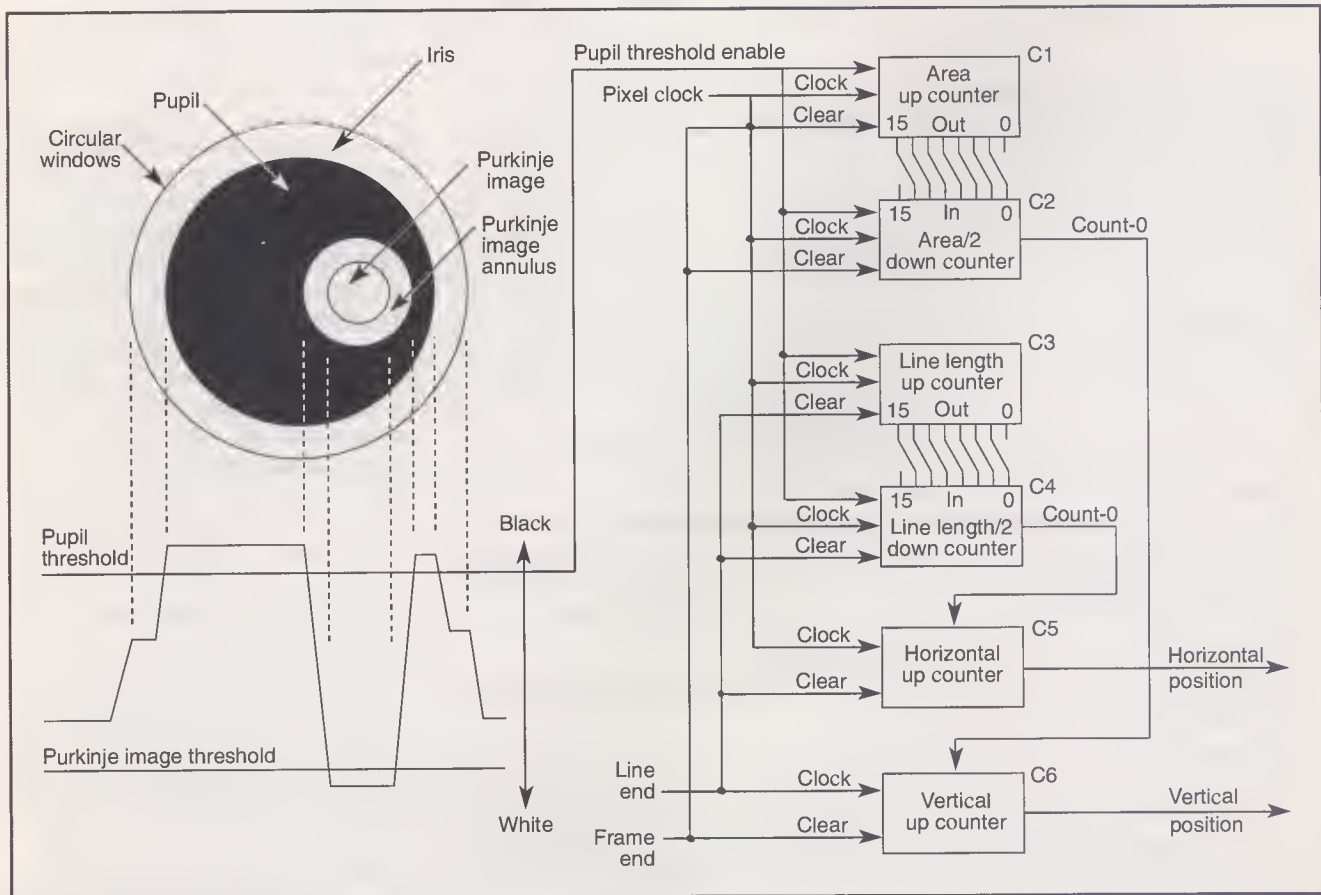


Figure 3. Detailed diagram of the thresholding and counter circuits. The left panel illustrates schematically the video field (rectangle) within which the tracking circular window (largest circle) is centered on the pupil (dark area). The First Purkinje Image (FPI, the brightest object in the image, is the specular reflection from the anterior surface of the cornea) lies in the lower right quadrant of the pupil, corresponding to an infrared light source below and to the right. The eye monitor hardware implements two thresholds, one to detect the dark pupil and one to detect the FPI. The counters (C1-C2) are enabled by the thresholded pupil signal and are either incremented or decremented by the CCD camera pixel clock. The digital switch strips out the synchronization pulses from the composite video and thresholds the video at two levels.

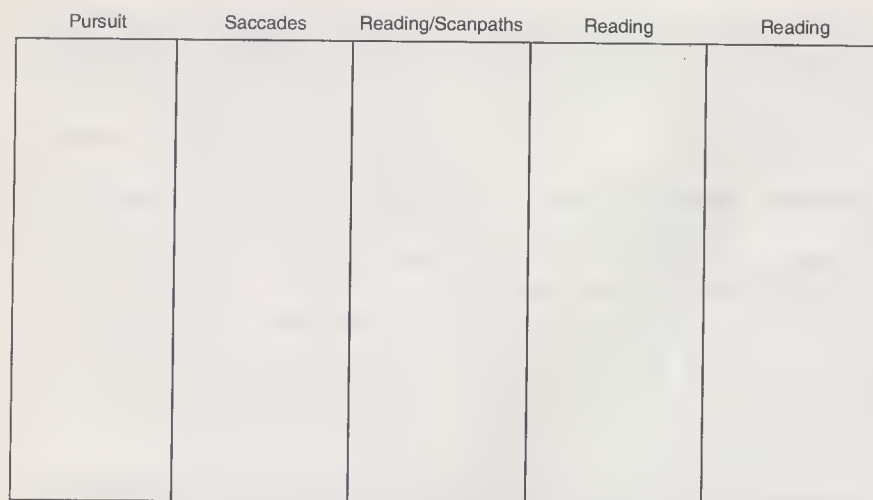


Figure 4. Typical eye movement recordings. The two panels at the right illustrate reading eye movements, showing the horizontal (rightmost panel) and vertical eye movements. The middle panel shows eye movements (with time implicit) of a subject reading Chinese (adapted from Sun, Morita, and Stark<sup>11</sup>). The two panels at the left display saccadic and smooth-pursuit eye movements as a function of time.

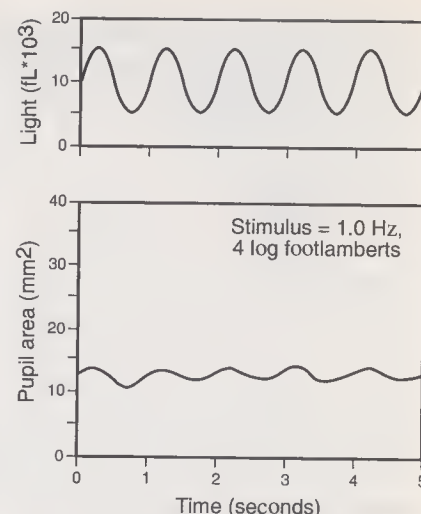


Figure 5. Pupillary movements in response to sinusoidal light stimuli. Note that the pupillary response is only approximately sinusoidal, illustrating the nonlinearity and noise present in the light-pupil reflex.

Table 1. Eye monitor performance.\*

| Eye movement measurements   |                                                                                                                               |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| Output (analog or digital)  | 12 significant bits                                                                                                           |
| Resolution                  | $\pm 0.2^\circ$ over $\pm 20^\circ$<br>$\pm 0.5^\circ$ over $\pm 45^\circ$                                                    |
| Head movements              | Fully compensated and linearized up to $\pm 3$ cm; larger range with reduced resolution                                       |
| Controls                    | Auto/manual mode switch<br>Pupil threshold (arrow keys)<br>Size and (in manual mode) position of circular window<br>Auto zero |
| Pupillometer                |                                                                                                                               |
| Output (analog or digital)  | 12 bits                                                                                                                       |
| Resolution                  | 0.02 mm <sup>2</sup> in area<br>0.01 mm in diameter                                                                           |
| Dynamic range               | 3 - 50 mm <sup>2</sup>                                                                                                        |
| Linearity                   | Within $\pm 0.1\%$ in area                                                                                                    |
| Temporal bandwidth          | Up to 60 Hz                                                                                                                   |
| Errors due to eye movements | Corrected to within 1% for eye movements up to $40^\circ$ horizontal, $30^\circ$ vertical                                     |
| Controls                    | Same as for eye movement measurements                                                                                         |

\*These performance specifications correspond to measurements of a subject sitting with his or her head in a chinrest, with head movement restricted to less than 3 cm in any direction. The camera views the subject's eye from straight ahead, at a distance of 0.6 m. The resolution of pupil size is diminished as allowed head movement excursion is increased, since the camera's field of view must be widened to accept these movements.

remented, in the same way that C1 was incremented, so that its contents are zero at the equator of the thresholded pupil. A counter (C3) clocked by the horizontal refresh pulse tracks the number of lines down from the top of the video image. Thus, the content of C3 at the end of a half frame is an uncorrected measure of the vertical position of the eye. The horizontal center of the pupil and the horizontal and vertical centers of the FPI are found in a manner conceptually similar to that for the vertical center of the pupil. The FPI is the brightest spot in the video image, and a second threshold comparator circuit is required (Figure 2).

Currently, the eye monitor uses a CCD camera and accesses pixels in raster order. Other schemes are possible, including random<sup>9</sup> access of pixels, use of other video technologies (for example, an earlier version of the system used an ultracon tube), or different video formats (for example, the European standard PAL<sup>10</sup>).

**Software.** The executive program is written in Turbo Pascal (Version 5.0), running under MS-DOS (Version 3.1 or later) on the Intel 80X86 processor family. It interrogates the user for information about the patient (name, ID number, diagnosis, etc.) and about the clinical paradigm (which eye is being stimulated, which eye is being recorded, stimulus type, etc.). It automati-

**Figure 6.** Photograph of the eye monitor in use in a clinical setting at the University of Iowa. The patient (left) sits with her head resting in a chinrest, which is part of an Allergan-Humphrey Visual Field Perimeter Testing System. The patient is wearing a pair of swim goggles, into which are mounted light-emitting diodes to provide both infrared light and visible light (as stimulus). The camera views her eye from behind the perimeter. The operator controls the eye monitor (which in turn provides voltages controlling the stimuli) by entering commands at the keyboard, and adjusts the potentiometers on the control panel. Above the control panel is the computer monitor, and above that are video monitors on which the raw and processed video are displayed. The eye monitor hardware resides in the IBM PC AT chassis, immediately below the keyboard. When the system is in use, the room is darkened, and a curtain is drawn between the operator and the patient so that stray light from the apparatus does not interfere with the stimulus.



cally calibrates eye movement measurements; then it delivers a preprogrammed stimulus signal (via a Data Translation 2801A D/A board) to control the stimulus apparatus, an LCD shutter backlit by a color video monitor. The assembly language routine Etrack, written in Microsoft Macro Assembler, is called by the executive. The first time it is called, it initializes the boards (setting all the counters to their initial values). It then begins searching for the pupil in the center of the screen, expanding window diameter until the pupil appears.

Figure 4 illustrates typical eye movement measurements. Figure 5 illustrates typical pupillary responses to sinusoidal light stimuli. Table 1 summarizes performance characteristics.

## Applications

The eye monitor has been developed continuously over about ten years. It is used worldwide for medical research into the mechanisms of night blindness, for clinical measurement of the integrity of the visual system, and for basic research into visual perception and eye-movement control mechanisms in health and disease. It is used to measure the eye movements of radiologists as they read X-rays to determine differences between novice and experienced readers. It is used to study the reading eye movements of dyslexics and to study children with amblyopia (weak eye) and strabismus (misaligned eyes). It is used to study the development of fatigue and

discomfort in computer VDT users. One measure of fatigue is the blink rate, which the system can measure.

The eye monitor is also being used in nonmedical applications. For example, the eye movements of paid subjects are measured while they view advertisements. By determining where the subjects look first and longest (at the pretty girl, the product, or the logo), it helps estimate an advertising campaign's effectiveness before millions of dollars are expended. Finally, it has been used as an "eye mouse" that lets computer users move the cursor by looking at the desired position on the screen and typing control-H. Thus, users can keep their eyes on the screen and fingers on the home keys (especially useful for touch typists) and eliminate the desktop clutter associated with a mouse and mousepad. It provides a fast, intuitive means of interacting with modern graphical user interfaces.

## Clinical example

The eye monitor system is being used at the University of Iowa for early clinical detection of visual diseases by objectively measuring pupillary responses to carefully controlled light stimuli (Figure 6).

**Measuring pupillary responses.** In the classic swinging flashlight test, a doctor swings a handheld penlight back and forth between the eyes. If one eye is weaker than the other (due, for example, to glaucoma, optic neuritis, tumor, stroke, or trauma), the responses of both pupils when the weaker

eye is stimulated are smaller and slower than when the normal eye is stimulated. This test depends on the physician's subjective judgement of the equality of responses and on the equality of the stimuli to the two eyes. The test is hard to perform in patients with dark irises, and it is usually only qualitative.

We have developed a method for detecting visual deficits earlier in their course, when they are more treatable. The eye monitor provides carefully controlled stimuli and measures pupillary responses quantitatively and objectively. Since the pupillary system is highly nonlinear and the gain depends on average pupil size, we use the phase of pupillary responses to sinusoidal light stimuli instead of the amplitude. Phase seems to be a more reliable indicator of visual integrity.

The patient is seated comfortably in a dimly lit room with his or her head supported by a chinrest. A fixation target minimizes eye movements and accommodation. Infrared light, invisible to the patient, illuminates the patient's eyes. The camera views the eye through a hole in a screen 0.6 meter in front of the subject. The screen provides a uniform gray field of about  $-0.5$  log footlamberts illuminance.

Sinusoidal light stimuli (1.0 Hertz) are presented in open loop mode using the compensatory feedback scheme described below. The luminance is initially 3.5 footlamberts. The phase of pupillary responses to stimulation of each eye is determined off line. To minimize the effects of spontaneous fluctuations in pupil size, only data with more than 95 percent coherence be-

tween stimulus and response are used to determine phase lag. If one eye is found to be weaker than the other (indicated by increased phase lag of the pupillary response to stimuli in the suspect eye), then the stimulus to the healthy eye is decremented in brightness in 0.1 log unit steps, until a match condition is obtained. The depth of the deficit is indicated by how much the stimulus in the stronger eye must be reduced to achieve equality of responsiveness in phase lag.

#### Opening the light-pupil reflex loop.

The light-pupil reflex is ordinarily a closed loop. Since the feedback is nonlinear (retinal illuminance is the product of pupil area and incident light flux), the system must be rendered open loop for effective study using the tools of engineering systems analysis. The computer provides electronic feedback based on measured pupil area to control stimulus intensity and thus compensate for changes in pupil size dynamically. This is accomplished by real-time simulation of an adaptive autoregressive moving average representation of the pupillary control system.<sup>12</sup> This method also implements a prediction scheme to compensate for delays in the measurement and stimulus apparatus. The resultant signal controls light flux so that the product of incident light and pupil area is equal to the desired value of retinal illuminance. The parameters of the model adapt so that the retinal illuminance equals the desired value. These parameters themselves provide an estimate of the visual system's integrity, which is being investigated for use as a diagnostic tool. None of these capabilities would be possible without computers.

## Computers in medical measurements

**Human factors.** Ease of use and reliability of data are important in any application, but especially in clinical measurements. Frequent calibration and adjustments of the apparatus are not feasible. The system must be very robust — that is, it must obtain high-quality data from a wide variety of patients, some of whom have neurologic or other diseases that make it difficult for them to maintain a fixed gaze with the head held still. Also, many patients wear thick corrective lenses or contact lenses and have small pupils due to disease or aging. Some eye monitors have difficulty obtaining reliable measurements of small pupils. It is not possible to simply zoom in

on the patients, since eye and head movements would carry the pupil out of the video field.

The eye monitor described here has been used to measure pupillary and eye movements in thousands of individuals, many with one or more of the above complicating factors.

Most operators can use the system effectively after 30 minutes of training. The computer makes the system easy to use by relieving the operator of many tasks. It provides preprogrammed square waves, sinusoids, or other waveforms to control stimuli. It turns the chart recorder on and off, stores data on hard disk, and provides for analysis and graphical review and editing of data. The circular tracking window can usually find the patient's eye and resume tracking a given patient following a break. The added hysteresis allows tracking and reasonably accurate measurements even when the subject moves in depth. Some other eye monitors, especially those depending on edge detection, require immobilizing the patient's head with restraining straps or by using a dental impression and bite bar. While these methods work well in a research laboratory with trained healthy subjects, they may disturb or frighten some patients.

Some patients are so anxious about the outcome of the test (fears of blindness or other neurologic disease), or afraid that the apparatus might hurt them, that maintaining fixation is virtually impossible. In these cases, brief light flashes are administered under computer control only when the subject is looking at the target. In some paradigms, where we want to map retina responsiveness, we need only track where the subject is looking and correct the retinal-locus estimate by incorporating both the intended retinal locus and the gaze angles (horizontal and vertical). If the subject is having difficulty, a simple but effective technique is to stop the test and let the patient rest a few minutes. The patient is told that the same test will be repeated. Since it didn't hurt the first time, the patient is usually confident that it won't hurt the second time. Often the results of the second test are much improved.

**Auto zero.** A simple but effective technique for redefining the zero position in eye movement measurements is to have the patient look at a fiduciary point (usually the center of the field of view) while the operator presses the auto zero button on the front panel. The software stores the current eye position as the zero position, which is

subsequently used in the correction algorithms. This allows the operator to compensate for head movements without recalibrating. This is useful in patients who have difficulty holding their heads upright. Rather than recording for hours, with frequent recalibration to obtain a few minutes of good data, we are able to re-zero the eye monitor on the fly, and obtain records relatively unaffected by fatigue.

**B**y using an internal model of the object of interest (the eye), we can locate, track, and measure the eye in spite of interfering noise and other complications. In developing this "smart" instrument, we were guided by our understanding of the human visual system.

We extended the application of internal models to detect potentially blinding eye disease by comparing the light responses of the pupil to those of a mathematical model. By adapting the model parameters to yield the same responses as the eye, we are beginning to diagnose eye disease by "diagnosing" the model. ■

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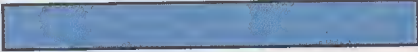
# A Microprocessor-Based Implantable Telemetry System

Kenneth W. Fernald, Todd A. Cook, Thomas K. Miller III, and John J. Paulos  
North Carolina State University

Using conscious, free-roaming animal subjects for biomedical research eliminates behavioral and physiological effects due to stress or anesthesia. To realize these benefits, biomedical researchers often use implantable systems to instrument and monitor the subject during testing. Unfortunately, commercial vendors do not supply flexible, inexpensive, implantable instruments. As a result, researchers must start from scratch to develop a short-term implant for laboratory use. This process leads to costly, protracted periods of development that make animal studies impractical for many researchers who would greatly benefit from them. This article introduces an attempt to eliminate the problem. It describes the design methodology and details of a flexible system that can meet the research requirements of a variety of biomedical applications, including cardiac studies, neurostimulation, and actuator control.

## General system requirements

Most implantable systems require high reliability, low power consumption, small size, and minimum weight. An application-specific design balances these requirements according to a particular set of needs. A more general system should allow the balance to be determined via software or



**This article describes the design methodology of an intelligent system for implantable biotelemetry instruments based on a modular set of CMOS chips connected by a specialized serial bus.**

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simple hardware changes that do not require a complete redesign effort. The result is a flexible system that can be configured for a wide range of experimental applications.

**Reliability.** System reliability is of great concern to biomedical researchers, particularly when they are dealing with human hosts. Because the proposed system is intended as a laboratory research tool for

animal studies and not as a means of providing long-term health support, this requirement can be relaxed somewhat. There are, of course, additional motives for providing a reliable system, including the temporal and monetary costs of system failure after implantation.

Implant failures can be divided into structural, environmental, and operational categories. Structural failures result from mechanical failure of components within the implant due to stress or fatigue. A common mechanism of this class is the failure of the bond wires on integrated circuits.<sup>1</sup> Environmental failures result from corrosion or damage due to the leakage of biological fluids into the implant package. Operational failures include the perturbation of transmitted data due to communication noise. Often the data obtained from the implanted device serve as input for decisions that can affect the health of the implant host. Error detection and data verification become critical issues for these types of systems.

**Battery lifetime.** Despite their limited capacity, batteries represent an excellent power source for implantable systems. Since power consumption scales roughly with the amount of work required of the implant, users must choose between battery lifetime and functionality. To provide maximum flexibility, this compromise should be reserved for the implant user,

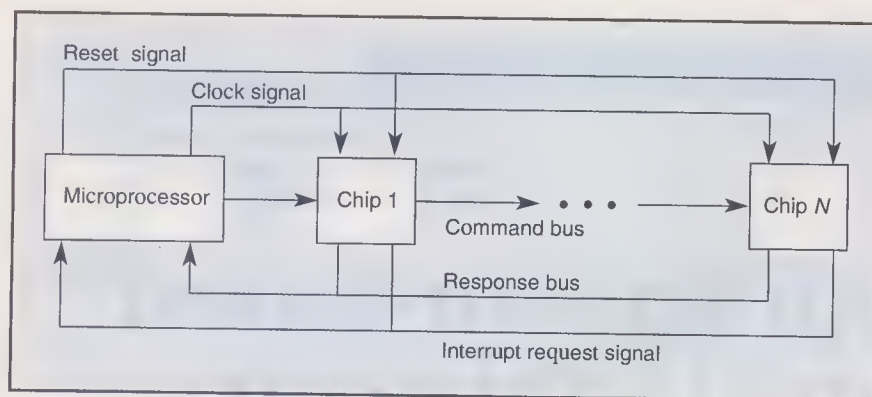


Figure 1. Basic system architecture for implantable instruments.

either via software control or simple hardware changes. This solution is most easily accomplished when the system can omit or power down unused components without affecting operation.

Lifetime also depends on battery size, which suggests a trade-off between lifetime and implant volume. The system should reserve the solution to this compromise for system users by supporting a battery technology that is available in a wide range of sizes. An excellent choice is a lithium-silver chromate battery with an open circuit voltage of 3.1.<sup>2</sup> This battery provides high power density while maintaining a nominal voltage over 80 percent of its lifetime.

**Size.** Implant volume requirements can differ greatly due to the size variations between different implant hosts (from mice to farm animals). To accommodate the obvious conflict between the implant's functionality and its size, the proposed system should allow the omission of components not required for a particular experiment. Note, however, that the implant volume depends more strongly on the packaging and battery size. For flexibility, the proposed system should conform easily to a variety of packaging techniques (such as hermetic cans and polymer sealants).

## System overview

The proposed system architecture, illustrated in Figure 1, consists of a modular chip set interconnected by serial command and response buses plus control signal lines.<sup>3</sup> A custom microprocessor serves as the bus controller and provides the flexibility necessary to satisfy a variety of application requirements. In addition to system configuration, functions such as information processing and closed-loop actuator control can be implemented via software.

Serial buses offer several advantages related to system requirements. First, the reduced signal count relative to parallel implementations improves system reliability and volume by lowering the number of wires required to connect the ICs. The elimination of address-decoding components also improves reliability and volume. The disadvantage of reduced throughput does not significantly impact system performance due to the low bandwidths (less than 1 kHz) typical of biological signals. This effect is even less critical when techniques are used to hide the latencies inherent in serial bus operation.

An additional advantage of serial buses is the ease with which the system can be expanded. Since all address decoding is

accomplished by bus protocol, any number of peripherals can be added to the system without redesigning existing components. This approach allows the quick prototyping of low-cost implantable systems using a common set of peripheral modules. For example, chips that perform data acquisition, actuator control, telemetry, or neurostimulation may be designed and used in a number of different implant systems as long as they implement the standard bus protocol.

## Serial bus design

Interchip communication occurs over two unidirectional serial buses and reset, clock, and interrupt-request signals, as shown in Figure 1.

**Command bus.** This bus originates at the microprocessor and serves as the path for commands issued to system peripherals. As a command frame is shifted onto the bus, it is examined by each peripheral and then passed on in a daisy-chain fashion.

All command frames consist of a combination of six possible fields: start bit, command, address, abort bit, data, and stop bit. Table 1 illustrates the five possible command frames, which are shifted onto the command bus from left to right. The address and data fields are both 16 bits and are transmitted with the least significant bit (LSB) in the first position. The functions of the abort bit and the Read and Write Buffer commands are discussed in the section on addressing.

**Response bus.** This bus is shared by all peripherals and returns the requested information from Read and Acknowledge Interrupt commands. Response frames consist of a start bit, a 16-bit data field transmitted LSB first, and a stop bit. Since peripherals share this common signal, each must disable its driver when not responding to a command. The address decoding of the bus protocol ensures that no two peripherals drive the response bus simultaneously.

Table 1. Serial bus commands.

| Command        | Bus Sequence |     |         |       |      |
|----------------|--------------|-----|---------|-------|------|
| Read Buffer    | 1            | 000 | ABORT   |       | 0    |
| Write Buffer   | 1            | 001 | ABORT   | DATA  | 0    |
| Read Register  | 1            | 010 | ADDRESS | ABORT | 0    |
| Write Register | 1            | 011 | ADDRESS | ABORT | DATA |
| Ack Interrupt  | 1            | 100 | ABORT   |       | 0    |

**Interrupt Request signal.** The peripherals and microprocessor share a wired-OR signal. A peripheral issues an interrupt by pulling this signal low and waiting for a valid Acknowledge Interrupt command, after which it returns an interrupt vector on the response bus. The microprocessor uses this

16-bit vector as the starting address of the appropriate interrupt service routine, thereby avoiding the overhead associated with a local vector table. The interrupt vector registers on each peripheral are written by the microprocessor during program initialization.

**Addressing.** Each peripheral's manipulation of the address field and abort bit in a command frame allows the microprocessor to address peripherals without additional decoding components. As the address field passes serially through each peripheral, it is changed by subtracting that peripheral's address space size from the received address. Since the address is received LSB first, this subtraction can be performed in a bit-serial fashion. This modified field is then passed to the next position on the daisy-chain in place of the original. If this subtraction results in a negative value (that is, the original address is within the peripheral's address space), the command is accepted by the peripheral, and the abort bit for that frame is set, forcing subsequent peripherals to ignore the command regardless of the address. This technique allows each peripheral's local address space to start at 0000H, so its design need not depend on a particular system configuration. Figure 2 is an example of the serial addressing scheme.

The main function of the abort bit is to reduce latencies associated with the daisy-chain bus. Rather than requiring each peripheral to accumulate a complete command frame (and determine if it is being addressed) before passing it down the chain, the abort bit allows passing a command frame between devices with a 1-bit delay. Only when a device has seen the entire address and determined that it was the intended recipient does it set the abort bit to notify subsequent devices of that fact. The daisy-chain also establishes interrupt priority by allowing the first peripheral that sees an Acknowledge Interrupt command to accept it by setting the abort bit, thus forcing other devices requesting an interrupt to wait for the next acknowledgment.

One disadvantage of this addressing technique is that the microprocessor does not know the address of the telemetry unit prior to programming. This problem is critical. Because all programming occurs through the telemetry link, the processor must know how to read the received bootstrap program without knowledge of the telemetry buffer's location in the system memory map. Although the microprocessor could require that the telemetry unit

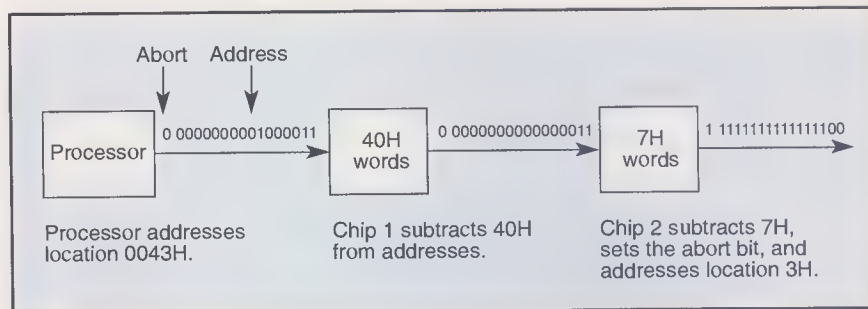


Figure 2. Example of the serial bus addressing scheme.

always be first in the command bus chain, this requirement would reduce the system's flexibility by forcing that unit to have the highest interrupt priority. Instead, special bus commands (Read and Write Buffer) provide access to the telemetry data buffer without an explicit address.

## Microprocessor design

The unique requirements imposed by implantable systems suggest that a custom microprocessor design is both desirable and appropriate.

**General requirements.** Algorithms typical of biomedical analysis (such as band limiting, data compression, or event detection) consist of heuristics combined with some form of vector calculation.<sup>4,5</sup> For example, the basic finite-impulse response (FIR) filter equation

$$y(t) = \sum_{n=0}^{N-1} a_n x(t - nT) \quad (1)$$

(where  $N$  represents impulse response

length,  $T$  sample interval,  $y$  filter output,  $x$  filter input,  $t$  time, and  $a$  filter parameter) is commonly used due to its linear phase characteristics. Such calculations are extremely common in signal processing algorithms, which suggests a need for instructions that implement them efficiently.

Additional microprocessor requirements include resetting peripherals, servicing interrupts, and controlling serial bus transactions and the system clock. To allow fast prototyping of a flexible research instrument, programming is through telemetry, either before or after the implantation. Thus, many experiments can be performed without physically altering the implanted system.

**Programmer's model.** The microprocessor is a 16-bit, general-purpose design based on the Hector microprocessor with several features added to support system requirements.<sup>6,7</sup> The processor has 14 general-purpose, 16-bit registers (plus the program counter and stack pointer), an 8-bit flag register, 39 instructions, 16 kilobits of static RAM, and an on-chip timer system. Table 2 lists the available status flags.

Table 2. Microprocessor status flag definitions.

| Flag     | Definition                                  |
|----------|---------------------------------------------|
| $I_{T0}$ | Masks interrupt from timer 0                |
| $I_{T1}$ | Masks interrupt from timer 1                |
| $I_E$    | Masks peripheral interrupts                 |
| $R$      | Set if a Repeat instruction is in progress  |
| $C$      | Contains carry out of arithmetic operations |
| $N$      | Set if ALU result is negative               |
| $V$      | Set if ALU operation overflows              |
| $Z$      | Set if ALU result is zero                   |

**Table 3. Microprocessor instruction-set summary.**

| Instruction |                                                 | Operation                                                                                                                            |
|-------------|-------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| Type        | Subtype                                         |                                                                                                                                      |
| Add         | Src,Dst                                         | Add source to destination                                                                                                            |
| Addc        | Src,Dst                                         | Add source and <i>C</i> flag to destination                                                                                          |
| And         | Src,Dst                                         | AND source to destination                                                                                                            |
| Btst        | Src,Dst                                         | AND source to destination to set <i>C</i> , <i>N</i> , <i>V</i> , and <i>Z</i> flag bits and discard result                          |
| Cmp         | Src,Dst                                         | Subtract source from destination to set <i>C</i> , <i>N</i> , <i>V</i> , and <i>Z</i> and discard result                             |
| Move        | Src,Dst                                         | Move source to destination                                                                                                           |
| Or          | Src,Dst                                         | OR source to destination                                                                                                             |
| Sub         | Src,Dst                                         | Subtract source from destination                                                                                                     |
| Subc        | Src,Dst                                         | Subtract source and <i>C</i> flag from destination                                                                                   |
| Xor         | Src,Dst                                         | XOR source to destination                                                                                                            |
| Smac        | Src,Src                                         | Perform signed multiply; accumulate it in registers <i>R0</i> and <i>R1</i> .                                                        |
| Bra         | Targ,CC                                         | If condition code is true, branch to target                                                                                          |
| Call        | Targ,CC                                         | If condition code is true, call subroutine at target                                                                                 |
| Smove       | Src                                             | Start a move from source                                                                                                             |
| Fmove       | Dst                                             | Finish a move to destination                                                                                                         |
| Sif         | Dst                                             | Store flags register into destination                                                                                                |
| Ldf         | Src                                             | Load flags register from source                                                                                                      |
| Dnzn        | Targ,Rn                                         | Decrement register <i>Rn</i> and branch to target if <i>Rn</i> = 0                                                                   |
| Push        | Src,Rn                                          | Push source onto stack pointed to by <i>Rn</i>                                                                                       |
| Shl         | Src,Rn                                          | Shift left with <i>Rn</i> as shift count                                                                                             |
| Shr         | Src,Rn                                          | Perform arithmetic shift right with <i>Rn</i> as shift count                                                                         |
| Rol         | Src,Rn                                          | Rotate left with <i>Rn</i> as rotate count                                                                                           |
| Ror         | Src,Rn                                          | Rotate right with <i>Rn</i> as rotate count                                                                                          |
| Addq        | #s4,Dst                                         | Add 4-bit signed constant to destination                                                                                             |
| Caddq       | #s4,Dst                                         | Perform one's complement of 4-bit signed constant added to destination                                                               |
| Cmpq        | #s4,Dst                                         | Compare 4-bit signed constant to destination                                                                                         |
| Movq        | #s4,Dst                                         | Move 4-bit signed constant into destination                                                                                          |
| Setf        | #m8                                             | Set flags according to 8-bit mask                                                                                                    |
| Clrf        | #m8                                             | Clear flags according to 8-bit mask                                                                                                  |
| Rti         | —                                               | Return from interrupt                                                                                                                |
| Rep         | Src                                             | Repeat next instruction with source as repeat count                                                                                  |
| Mulu        | <i>Rn</i> <sub>1</sub> , <i>Rn</i> <sub>2</sub> | Perform unsigned multiply with result in <i>R0</i> and <i>R1</i>                                                                     |
| Divu        | <i>Rn</i> <sub>1</sub> , <i>Rn</i> <sub>2</sub> | Perform unsigned division of <i>Rn</i> <sub>1</sub> by <i>Rn</i> <sub>2</sub> ; place quotient in <i>R0</i> , remainder in <i>R1</i> |
| Muls        | <i>Rn</i> <sub>1</sub> , <i>Rn</i> <sub>2</sub> | Perform signed multiply with result in <i>R0</i> and <i>R1</i>                                                                       |
| Divs        | <i>Rn</i> <sub>1</sub> , <i>Rn</i> <sub>2</sub> | Perform signed division of <i>Rn</i> <sub>1</sub> by <i>Rn</i> <sub>2</sub> ; place quotient in <i>R0</i> , remainder in <i>R1</i>   |
| Sleep       | —                                               | Put processor into low-power sleep state                                                                                             |
| Reset       | —                                               | Send reset signal to external devices                                                                                                |

Table 3 summarizes the full instruction set. The Repeat and Signed Multiply-Accu-

mulate instructions and the auto-increment addressing modes provide support

for the biomedical calculations we discussed. Rep repeats the next instruction a given number of times. It can be used with the arithmetic instructions to perform element-by-element operations on vectors and with Smac to perform the accumulated product calculations found in Equation 1. Since auto-incrementing of pointers is available, implementing FIR filters and similar calculations uses very little code space.

The microprocessor supports the serial buses with several features that attempt to hide the latencies of bus transactions. The most important feature is the on-chip SRAM, which lessens crossing the serial bus for instructions and data. Serial bus support also includes buffering of bus transactions by latching each command into a parallel-to-serial shift register, allowing the processor to proceed while the command is shifted onto the bus. Serial bus reads may also be pipelined using the Start Move and Finish Move instructions. Smove starts a serial bus read and allows the processor to continue program execution until the requested data are required, whereupon Fmove waits for the transaction to complete.

The microprocessor contains two on-chip, programmable timers that can be used for such periodic tasks as data sampling. Each timer is free running and counts from a preset value down to zero, issues an interrupt, and reloads its programmed value. Both timer interrupts are individually maskable using the *I*<sub>70</sub> and *I*<sub>71</sub> bits of the flag register. For a processor clock rate of 10 MHz, timer intervals from 0 to 6.5 milliseconds can be obtained.

Using an SRAM peripheral expands memory for field studies in which the test subject must be captured or retrieved. In such instances, the implant stores relevant sensor information over several days and transmits that data when requested by a telemetry command. This extended memory could also provide program storage if pages were overlaid into the local RAM before their execution, although the obvious speed constraints would limit such paging to infrequently called routines.

## Telemetry design

Here we describe the bidirectional telemetry chip that performs all external communications.

**Functional model.** The microprocessor maintains complete control of the telemetry

unit (illustrated in Figure 3) by using the serial bus interface common to all peripherals. The processor may instigate a transmission by writing data into the telemetry FIFO (first-in, first-out) stack and then writing a value to the command register.

The telemetry unit has several registers that allow the processor to control and monitor the unit's operation. The most important of these are the command register and the control/status register pair (see Figure 3 and Table 4). The available status information indicates

- whether the unit is currently transmitting or receiving,
- the status of the four interrupts,
- the reset state of the FIFO, and
- overflow, check-sum, time-out, and bus-error bits.

An overflow error occurs when new data are received before the previous Receive Complete interrupt signal has been serviced. A bus error results when the processor attempts to read or write the FIFO during a transmission or reception. Detailed status bits are also available for system verification and hardware failure detection. The control register provides enable/disable bits for the four interrupts and a bit to reset the data FIFO.

The interrupt signals issued by the telemetry unit are Receive Complete, Transmit Complete, Error, and Timer. The first two interrupts mark the ends of successful receptions or transmissions, thereby informing the processor either that new information is available in the FIFO or that the unit is now available for the next operation. The Error interrupt occurs when the system detects check-sum, time-out, or bus errors. The FR status bit (see Table 4) can determine if an error destroyed the FIFO contents (for example, receiving an incomplete data field). The final interrupt is associated with a programmable timer that lets the microprocessor terminate a Sleep instruction after a preset interval.

Since the microprocessor is booted through the telemetry unit, the FIFO must be large enough to contain a reasonable bootstrap routine. For example, the routine may move itself into high memory and then load the system program from the telemetry unit into low memory. The program would be received in FIFO-sized segments. Upon completion of this operation, the bootstrap routine would transfer control to the appropriate memory location. A 64-word FIFO provides ample memory for

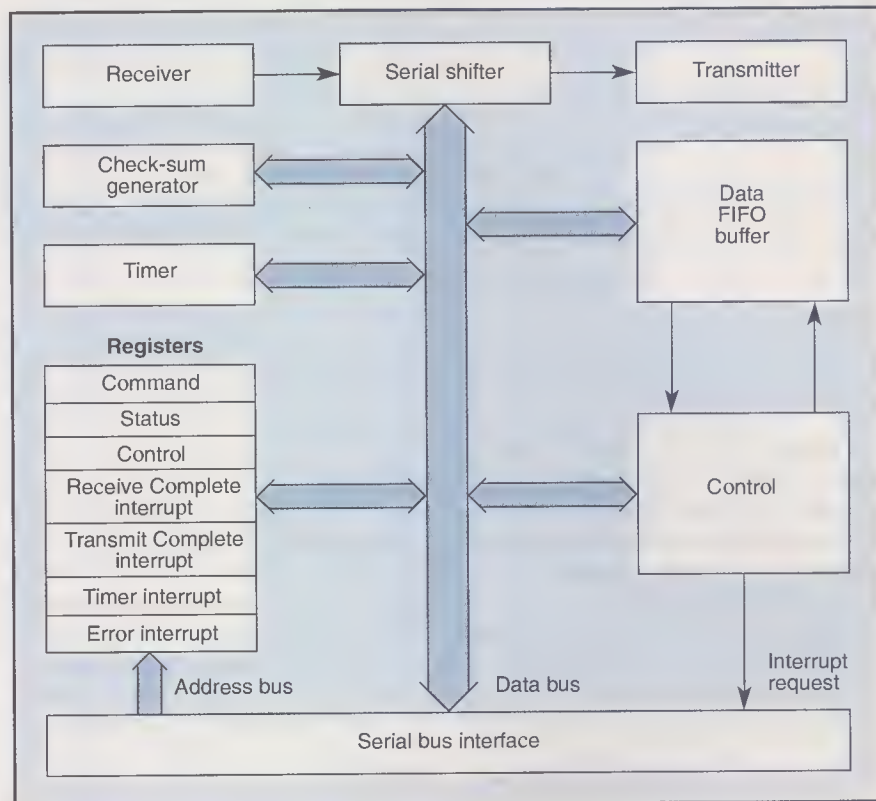


Figure 3. Block diagram of the bidirectional telemetry unit.

Table 4. Telemetry control and status registers.

| Bit            | Telemetry control                               |
|----------------|-------------------------------------------------|
| RF             | Reset FIFO                                      |
| $I_E$          | Mask Error interrupt                            |
| $I_M$          | Mask Timer interrupt                            |
| $I_T$          | Mask Transmit Complete interrupt                |
| $I_R$          | Mask Receive Complete interrupt                 |
| Bit            | Telemetry status                                |
| $C_{on}$       | Set when receiver is listening                  |
| $Q_A$ to $Q_D$ | Hardware state information                      |
| FR             | Set when FIFO has been reset                    |
| $E_O$          | Indicates an overflow error                     |
| $E_B$          | Indicates a bus error                           |
| $E_C$          | Indicates a check-sum error                     |
| $E_T$          | Indicates a time-out error                      |
| $I_{EP}$       | Set when Error interrupt is pending             |
| $I_{MP}$       | Set when Timer interrupt is pending             |
| $I_{TP}$       | Set when Transmit Complete interrupt is pending |
| $I_{RP}$       | Set when Receive Complete interrupt is pending  |
| TX             | Set when transmitting                           |
| RC             | Set when receiving                              |

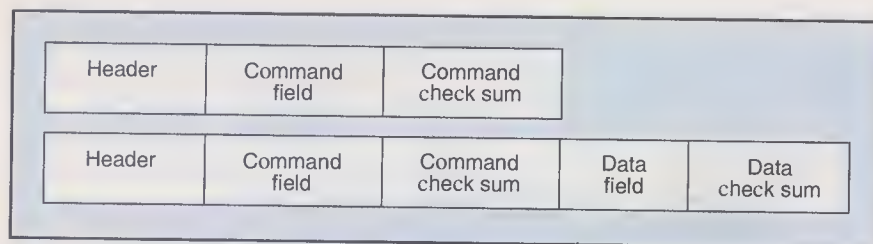


Figure 4. Two possible transmission/reception frames for the telemetry protocol.

these functions with room left for application-specific requirements.

**Circuitry.** A radio frequency carrier of about 40 MHz transmits and receives over a single coil antenna. This frequency meets the Federal Communication Commission's biomedical telemetry standard.<sup>8</sup> Transmission uses phase-shift keying on a continuous RF carrier with an average data rate of 100 kilobits per second (the actual rate varies with data content). To achieve high power efficiency, the transmitter must operate at the resonant frequency of the tuned antenna. A voltage-controlled oscillator searches for this frequency at the start of each transmission. This approach not only guarantees maximum power efficiency but also allows for both VLSI-process and antenna variations. A simpler pulse-width modulation scheme is adequate for reception because the external transmitter has plenty of power to deliver a strong signal to the receiving coil.

**Telemetry protocol.** Each transmission block to or from the telemetry unit contains five possible components: a header, command field, command check sum, data field, and data check sum, as illustrated in Figure 4. The transmission header is a period of unmodulated carrier approximately 80  $\mu$ s in length, allowing the external receiver time to detect the carrier prior to the start of data flow. The receive header consists of a series of 0s approximately 3 ms long fol-

lowed by a single 1 (a start bit). This unusually long receive header alerts the telemetry unit to the upcoming transmission. To conserve power, the receiver circuitry is activated only once every 3 ms. If no carrier is detected, the receiver is turned off immediately; otherwise it remains active until the telemetry transaction is complete. Since the receiver is off most of the time, a header length of at least 3 ms is required to ensure recognition of the transmission. However, the receiver is turned on immediately after each transmission for fast handshaking without requiring the 3-ms header.

The command field allows the implant system to exchange 14-bit command or status information with an external control station. This field is actually 16 bits long, but two bits are predefined by the telemetry protocol. The most significant bit (MSB) indicates whether that transmission contains a data field and data check sum. This allows transmission of either a single command or a command followed by a 64-word data/program block. The second MSB indicates whether the data field represents a bootstrap routine for the microprocessor. If this bit is set, the telemetry unit asserts a microprocessor reset operation and waits for the bootstrap routine to be requested. This bit has no predefined meaning for outgoing transmissions.

The command field is followed by a 16-bit check-sum value, the optional data field, and its 16-bit check sum. Words transmit LSB first. To allow the protocol to accommodate a large number of handshaking schemes, single-word commands may be transmitted and received without destroying the FIFO's contents. Without the command check sum, a corrupt MSB would cause FIFO loss even if no data field was actually present. Thus, command field contents must be verified before resetting the FIFO for a new data field. Unfortunately, we did not recognize this need until the telemetry design was nearly complete. To minimize the necessary changes, we added a second check sum instead of a single

parity bit. Although a full 16-bit check sum is excessive, it requires no additional hardware and helps prevent unintentional system reset operations by a malformed command field.

**Error detection.** Because of their hardware simplicity and reliability, we use 16-bit check-sum values to detect errors. During transmission or reception of a command field or data field, each 16-bit value is added to a check-sum register, producing a modulo- $2^{16}$  result. This result is modified by complementing all but the MSB before passing it to the transmit circuitry.

To understand the rationale for leaving the MSB uncomplemented during transmission, consider the following scenario. If an extra bit should appear at the beginning of the data block during a serial transmission of information (or if the first bit of the block is not recognized), each data word would be shifted either left or right by one bit. Depending on the actual data, this could be equivalent to multiplying or dividing the entire block by a factor of two. Since the check sum would also be modified by this same factor, there is a nonzero probability that the new data and the new check-sum value would still correspond and no corruption would be detected. Complementing the check-sum value has no effect since this error would simply modify its negative (one's complement) by a factor of two. However, by leaving the MSB of the check sum uncomplemented, a bit shift no longer corresponds to a multiply or divide operation, and the error is easily detected. A simulation that uses random data and generates several different classes of errors (single- and double-bit, and left and right frame shifts) has shown this detection scheme to be extremely effective in detecting transmission errors (see Table 5).

## Sensor interface design

The first sensor interface peripheral we designed for this architecture was a programmable signal-conditioning and acquisition chip intended for bio-potential studies. As Figure 5 shows, the chip provides eight differential analog input channels. These channels are compatible with a variety of sensors, including strain-gauge bridges and resistive transducers. Each channel contains a programmable gain stage that provides full-scale input ranges from  $\pm 5$  to  $\pm 100$  mV. The amplified signal is then band limited to a programmable frequency between 150 Hz and 10 kHz, after

Table 5. Error analysis results of telemetry check-sum scheme.

| Error Type        | Percentage of errors detected |
|-------------------|-------------------------------|
| Single-bit errors | 100                           |
| Double-bit errors | 96.9                          |
| Frame shifts      | 100                           |

which it is multiplexed into a 10-bit analog-to-digital converter. The resulting digital samples are stored in small FIFOs until they are read by the microprocessor. This is usually triggered by a FIFO Full interrupt issued by the sensor interface chip. To accommodate higher rates, the digital samples can be stored and read in pairs by packing the eight MSBs of two samples into a single serial bus response. This allows the user to compromise precision for speed when appropriate. Similarly, very slow sample rates (and possibly higher resolution) may be achieved by oversampling and averaging the acquired data.

## Clock requirements

In CMOS designs, most power consumption results from the charging and discharging of capacitive loads, the largest of which are the interconnect wires between ICs. Because the system clocks are usually the fastest signals in a digital design, their distribution is critical for low-power operation. In our system, the microprocessor, the serial buses, and various peripheral chips each require a clock to operate.

**Microprocessor.** As in any digital design, the optimal clock frequency depends on the amount of processing to be performed and the number of clock cycles that processing requires. To determine the necessary clock speed for various applications, we implemented several biomedical algorithms by using the instruction set in Table 3. For example, a routine that processes and transmits  $M$  channels of sampled input using identical FIR filters of order  $N$  resulted in the following equation for the number of clock cycles required per sampling period:

$$T \approx 120M + 20MN$$

The first term accounts for the overhead of bus transactions and subroutine calls, while the second term represents the time actually used for multiply-accumulate instructions during filter calculations. If the routine was attempting to process eight channels of input at a sampling rate of 1 kHz per channel using a 10th-order filter (typical values for implant systems), a 2.6-MHz clock frequency would be required. Higher clock rates would accommodate more ambitious algorithms (our target clock specification is 10 MHz).

**Serial bus.** The lower limit of the bus clock frequency depends on the bus

throughput required. Since most bus data originate from sensor inputs, this throughput is approximately the total sampling rate expected for these applications. Except for neural potentials, nearly all biological signals have bandwidths below 1 kHz. Assuming that some applications may require 16 or 24 channels of input (neglecting the obvious packaging challenge) sampled at a Nyquist rate of 2 kHz, a bus throughput of up to 48 Kwords per second would be required. Given that a Read Register command requires 40 bus clock cycles (including the response time), the total required clock frequency would be almost 2 MHz.

**Peripherals.** The clock requirements of future peripherals are difficult to determine without knowing their exact applications. Given the context of an implantable system, those applications can generally be characterized as either sensing biological signals or generating actuator control signals. This suggests that the signals of interest to most peripherals are less than 10 kHz in bandwidth. Since analog process-

ing circuitry (switch-capacitor filters in particular) sample signals at 10 to 20 times their Nyquist sampling rate, this implies a maximum operating frequency of approximately 0.5 MHz.<sup>9</sup> Note that these circuits typically require a continuous clock for proper operation.

**Clock distribution.** Techniques for system clock distribution and control can be classified as either centralized or decentralized. Centralized clock schemes use a set of clock networks under the control of a single unit, usually the microprocessor. Each network attempts to satisfy a unique set of clock requirements. In the proposed system, the microprocessor would maintain one continuous, low-frequency (0.5-MHz) clock for peripherals and a second high-speed (2-MHz) clock that is active only during bus transactions. Each clock would be derived from a common clock oscillator and qualified with digital logic prior to distribution. Unfortunately, digital signal distribution is inefficient due to the charging and discharging of capacitive clock loads. Assuming the bus operates around

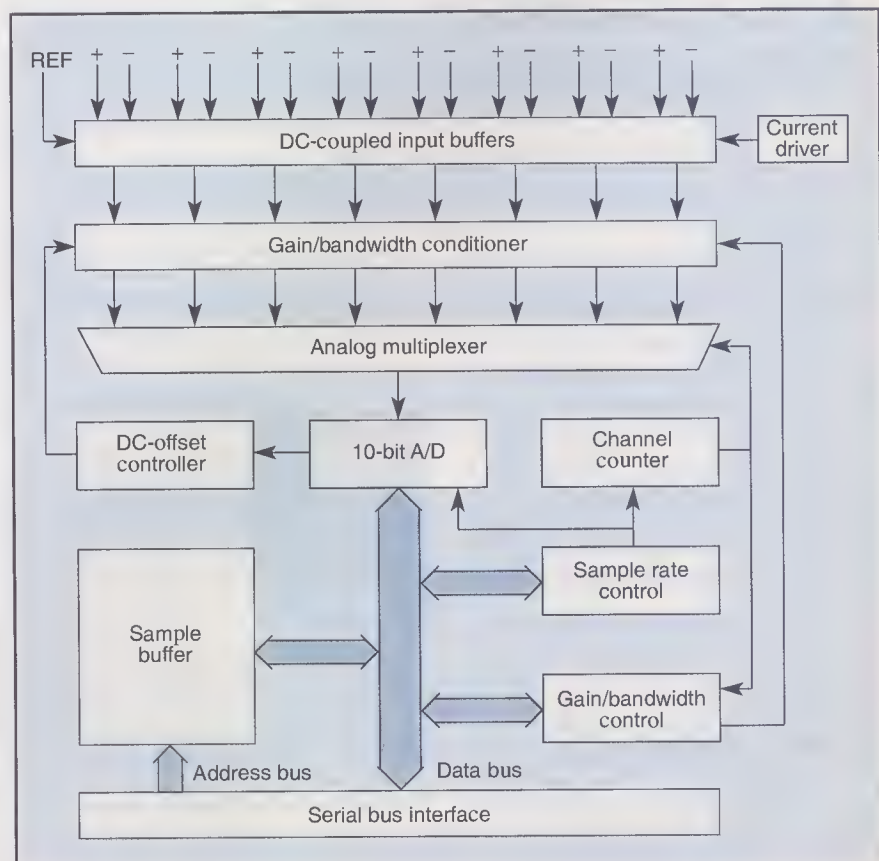


Figure 5. Block diagram of the sensor interface peripheral.

50 percent of the time, the resulting current drain would be approximately 135 mA if each clock network has a capacitance of 30 pF.

This high current drain can be eliminated by a decentralized technique in which one continuous clock satisfies bus and peripheral requirements. Each peripheral is made responsible for any additional clock conditioning required for its own function. The effects of capacitive loading on this high-frequency clock can be nearly eliminated by incorporating the load as part of a sinusoidal crystal oscillator circuit. The motional inductance of the crystal resonates with the load to produce a purely reactive circuit, thus eliminating nearly all power consumption associated with clock distribution. The main disadvantage of this technique is an increase in interchip clock skew due to the slow rise and fall times of the resulting signal. This skew can be reduced somewhat by distributing a differential clock signal and placing differential comparators on each chip. We chose the sinusoidal clock distribution for its excellent flexibility and power characteristics.

**T**he proposed architecture addresses the requirements of low power, small size, and high reliability through the use of a modular set of CMOS chips interconnected by a specialized serial bus. This approach supports the fast, inexpensive prototyping of research instruments using a common peripheral chip set. The telemetry unit has been fully fabricated and tested with excellent results. The microprocessor and sensor interface chips are in the design stage and should be available for fabrication in early 1991.

The initial application of this system will be accomplished through the National Science Foundation Engineering Research Center (ERC) for Emerging Cardiovascular Technologies at Duke University. The ERC hopes to facilitate the use of telemetry in conscious animal studies by providing both hardware and application support to other biomedical research laboratories. ■

## Acknowledgments

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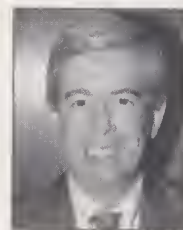
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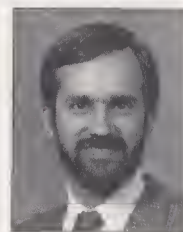
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# The Fifth International Parallel Processing Symposium

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# Parallel Processing for Biomedical Signal Processing

## Higher Order Spectral Analysis — An Application

Elias S. Manolakos, Haris M. Stellakis, and Dana H. Brooks

Northeastern University

**M**edical practitioners are increasingly using computer-based medical systems to collect, store, and process digitized biological signals.<sup>1</sup>

The signals they collect and process via these systems include bioelectric potentials, such as those generated by the heart (ECG or electrocardiogram), brain (EEG or electroencephalogram), or skeletal muscles (EMG or electromyogram). Such signals include nonelectric signals that might be transduced and then recorded (for example, breath sounds or speech waveforms), and biomedical images from ultrasound, X-ray, CAT scan, MRI, etc.

These signals are often interpreted heuristically by medical practitioners, and the need for sophisticated algorithms for processing, coding, and automatically interpreting the information these signals contain is increasing.<sup>1</sup> Among the advantages of automated processing are objectivity, reliability, repeatability, and speed. Of course, as biomedical signal processing algorithms gain sophistication, more computational resources are needed, while most biomedical signal processing must be done in or near real time.

The volume of data is often high, computational resources are often scarce, and



**The transition from  
uniprocessor to  
multiprocessor  
architectures is  
mandated to achieve  
real-time performance  
in computer-based  
medical systems for  
biomedical signal and  
image processing.**

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the cost of resources and computing time is important.<sup>1</sup> Thus, it is necessary to simultaneously consider not only whether a particular technique is useful but also how it might be efficiently mapped to special-purpose hardware to be included in a computer-based medical system (CBMS).

The power spectrum, the fast Fourier transform (FFT) of the autocorrelation of a

signal, is used widely to process biomedical signals. Power spectrum estimation and analysis is one of the most common, well-developed, well-understood, and useful tools of digital signal processing (DSP).

The roots of this field go back beyond this century, but the past 25 years has seen an explosion in the development, analysis, and application of power spectrum techniques. Many methods for estimating and analyzing power spectra have been applied to the types of biomedical signals likely to be recorded by a CBMS. (For a detailed discussion of power spectrum estimation in the context of biomedical signal processing, see Childers.<sup>1</sup>)

Almost any current publication with articles on biomedical signal processing contains details of new research or clinical applications of power spectrum analysis. For instance, 10 of the 16 articles in a 1990 special issue of *IEEE Engineering in Medicine and Biology Magazine* devoted to biomedical signal processing<sup>2</sup> involved applications of power spectrum techniques.

Why are power spectra so extraordinarily popular and useful to biomedical signal processors? First, power spectra are easily understood to have physical significance, for example, in terms of the power of the

## Glossary

|          |                                                      |
|----------|------------------------------------------------------|
| CBMS     | Computer-based medical system                        |
| CMM      | Canonical mapping methodology                        |
| CAT scan | Computerized axial tomography                        |
| DG       | Dependencies graph                                   |
| ECG      | Electrocardiogram                                    |
| EEG      | Electroencephalogram                                 |
| EMBS     | The IEEE Engineering in Medicine and Biology Society |
| EMG      | Electromyogram                                       |
| GMM      | Generalized mapping methodology                      |
| HOS      | Higher order spectra                                 |
| LRA      | Locally recursive algorithm                          |
| Mac      | Multiply-accumulate computation                      |
| MRI      | Magnetic resonance imaging                           |
| SAF      | Single assignment form                               |
| SFG      | Signal flow graph                                    |
| SNR      | Signal-to-noise ratio                                |
| STI      | Structurally time-invariant                          |
| TI       | Time-invariant                                       |
| WSI      | Wafer scale integration                              |

original analog signal at the corresponding analog frequency. Second, the large number of power spectrum estimation algorithms makes it possible to analyze a wide variety of biomedical signals. Third, because many biomedical signals have dominant frequency components,<sup>1</sup> power spectra might often compress, highlight, or extract information in a signal that can be difficult or impossible to locate directly from the signal. Fourth, power spectra are relatively computationally efficient.

Like any DSP technique, power spectrum estimation has limitations and disadvantages for use on biomedical signals. To overcome some of these limitations, many DSP researchers have been exploring in the past few years a generalization of power spectra termed higher order spectra.<sup>3</sup> HOS have been applied on a number of real-world problems, including biomedical signal processing.<sup>2,4</sup>

HOS are defined, analogously to power spectra, as multidimensional Fourier transforms of the higher order correlations (more precisely of the higher order *cumulants*) of a signal. In the past few years, a significant amount of work has been done developing HOS theory and applications. (For an excellent tutorial presentation with extensive references, see Nikias and Raghuveer.<sup>3</sup>)

The particular higher order spectrum with which we deal here is the third-order spectrum, known as the *bispectrum*, which can be defined as the 2D Fourier transform of the third-order cumulant (or moment) sequence. With HOS, we can extract

medically significant information not available in the power spectrum.

As yet, medical applications of HOS are mainly confined to research studies, but there is good reason to expect more interest soon in clinical applications. However, HOS are significantly more computationally intensive than power spectra. Thus, our ability to exploit the power of HOS for processing signals acquired by a CBMS is inextricably linked to our ability to compute HOS efficiently.

To illustrate the motivation for using HOS, we describe three limitations of power spectra. We show how these limitations are serious problems for biomedical signal processing and how HOS can provide solutions.

First, power spectra are always minimum phase spectra; that is, they might be insensitive to the true phase of a signal. They are not unique, in the sense that there might be many different signals with the same power spectrum and the phase information of a nonminimum phase signal is lost. Second, power spectra are insensitive to nonlinearities in a signal. Third, power spectra are sensitive to Gaussian observation noise.

HOS have an advantage over power spectra to the extent that each can represent the true phase of a signal.<sup>3</sup> Unlike power spectra, HOS, including bispectra, preserve the true phase information of a signal except for a linear phase factor (that is, a time shift).

Many biomedical signals are nonminimum phase, and phase information in a

signal (related to the timing of events) is often the most important information.<sup>5</sup> In addition, nonminimum phase information might distinguish between two signals that have identical power spectra.

Signal averaging is also extremely important in biomedical signal processing.<sup>1</sup> It is used on many biomedical signals (such as EEGs and ECGs) to improve signal-to-noise ratio (SNR) and reduce variance. A serious problem for averaging is time registration, that is, unknown linear phase shifts. Averaging in the bispectrum domain should be possible, taking advantage of high SNR (suppression of Gaussian noise — see below) and preserving true-mixed phase characteristics while suppressing linear phase shifts.

Another important problem is the detection of nonlinearities that are manifested as phase coupling between harmonically related sinusoids. Phase coupling might reflect important interactions or relationships between physiological processes. For instance, there has been particular interest in detecting phase coupling in EEGs (to measure depth of anesthesia and to understand relationships between different frequency bands and vigilance states and between EEG changes in the right and left brain hemispheres as related to conceptual processes<sup>2,4</sup>). The same holds true in ECGs, where phase coupling has been linked to interactions between the two parts of the autonomic nervous system.<sup>6</sup>

The powerspectrum is identical, whether or not phase coupling exists.<sup>3</sup> The bispectrum, on the other hand, detects phase coupling, thereby discriminating linear from nonlinear systems.

A third advantage of HOS is that, for Gaussian processes, all spectra of orders greater than two are identically zero.<sup>3</sup> One consequence for biomedical signals is that, if a signal is contaminated with Gaussian measurement noise, higher order spectrum domains might become high SNR domains. Thus, the bispectrum is often more robust to measurement (or other Gaussian) noise than the power spectrum.

Clearly, biomedical signals are subject to measurement noise, usually well modeled as being Gaussian and, thus, can benefit from this HOS property. This has been reported, for instance, when estimating spontaneous synaptic firing rates and parameters of individual muscle motor units from EMGs.<sup>4</sup>

HOS can also measure deviations from Gaussianity. Considerable work has been done studying the statistical properties of EEGs in particular. Bispectra have been

applied to characterize various vigilance states from EEGs in terms of the extent of deviation from Gaussianity.<sup>2,4</sup>

Given these HOS advantages, what are their disadvantages for use on biomedical signals compared to power spectra? One disadvantage is that HOS are more difficult to understand intuitively and interpret physically. Another is that HOS tend to need more data than power spectrum estimation techniques to have equal variance, and thus might be more sensitive to non-stationarities. However, recent developments in HOS research have gone a long way toward making HOS better understood, more widely employed, and more practical.<sup>3</sup>

A third disadvantage, which is particularly relevant here, is that HOS require significantly more computations than power spectrum techniques, especially in the estimation of the higher order cumulants. In particular, biomedical use of HOS requires some form of parallel processing and the development of special-purpose multiprocessor architectures.

In this article, we describe how systematic mapping methodologies can be used to derive special-purpose processor arrays for the estimation of the bispectrum via the third-order moments. We propose a novel design that is optimal in terms of total execution time for multiple pipelined blocks of data. Furthermore, we show how formal verification of the design can be achieved analytically.

## Mapping regular algorithms to parallel architectures

The problem of how an array architecture can be systematically derived given a regular algorithm has been a hot research topic for a decade. Many graph theoretic and algebraic mapping methodologies have been developed, stemming from the early work of Karp, Miller, and Winograd in 1967.<sup>7</sup>

The main idea is to write the algorithm in a suitable recursive form that captures its space-time activities and reveals potential parallelism. Then, you can follow well-defined transformation steps to produce different array structures, depending on desired optimality criteria.

Numerous authors have made important contributions in this field. Among them are Moldovan,<sup>8</sup> Rao and Kailath,<sup>9</sup> and Kung.<sup>10</sup> Some software tools that attempt to automate the mapping procedure have been

proposed.<sup>11,12</sup> These tools attempt to provide the front end of a silicon compiler to design a special-purpose multiprocessor tailored toward DSP applications. However, the tools are still immature and have not achieved global recognition.

In this article, we use the canonical mapping methodology that Kung introduced.<sup>10</sup> CMM has been used to derive arrays for a large number of DSP algorithms, such as convolution, filtering, band matrix multiplication, LU decomposition, QR factorization, etc. CMM is a subset of the generalized mapping methodology (GMM),<sup>10</sup> which can deal with nonregular algorithms that also consider the possibility of nonlinear assignment and nonlinear scheduling policies. The CMM decomposes into

- Stage 1: From the algorithm to the dependencies graph.
- Stage 2: From the dependencies graph to the signal flow graph (SFG).
- Stage 3: Array processor design.

*Stage 1:* To solve a problem, we first derive a recursive algorithm in single assignment form (SAF), in which every variable is assigned a value only once. If variables exist that need to become available across different recursions (global variables), they are localized by conversion to transmittant ones, before distribution among the recursions. A recursive algorithm with localized variables is called locally recursive. When an LRA is transformed to an array architecture, avoiding data broadcasting is guaranteed, and data movements are confined among neighbor processing elements (PEs). This is very desirable for a VLSI/WSI (wafer scale integration) implementation. Most algorithms commonly used in DSP applications have LRA expressions. However, important exceptions exist, including FFT and others that do not have equivalents in the LRA class.

There is a one-to-one correspondence between the LRA and the localized dependency graph. The DG is an acyclic-directed graph where nodes reside on the grid points of the LRA's index space; each one represents a computation instance. The arcs depict precedence relations (data dependencies) among computations that have to be respected if the algorithm is to be performed correctly by any underlying computer architecture. The DG is called homogeneous if each node models the same type of operation (for example, multiply-accumulate) and shift invariant if the node's edge structure is independent of the node's

position in the grid. The CMM can transform regular algorithms with homogeneous shift invariant DGs to systolic/wavefront array structures. It also can be extended to more general semiregular algorithms.<sup>10</sup>

*Stage 2:* An SFG is a directed graph where nodes represent computational stations and edges communication links. Timing is modeled explicitly by edge delays. The SFG can serve as an abstraction of the processor array. Hence, it can model the space-time realization of an LRA, providing both functional and structural information.

The functional SFG description defines the set of operations to be performed within the array node, and the structural description specifies the communication architecture (topology and relative delays). Using the CMM, a regular algorithm can be transformed to an SFG that remains structurally and functionally time-invariant (TI). On the other hand, semiregular algorithms with nonhomogeneous DGs could lead to structurally time-invariant (STI) SFGs, where the node's functionality could change with time.

To obtain an SFG from the DG, the following linear transformations should be applied:

- The nodes assignment, which maps a set of DG nodes (modeling computations) to a particular SFG node (modeling a processing element or PE).
- The nodes scheduling, which maps a DG node to an integer, corresponding to the schedule time period of execution. All DG nodes executed at the same schedule time (but in different SFG nodes) belong to the same equitemporal hyperplane. Therefore, scheduling imposes an ordering to the set of DG nodes assigned to an SFG node.

*Stage 3:* In this stage, the SFG is transformed to either a globally synchronous systolic array or to an asynchronous data-driven wavefront array. The transformation is not unique. Techniques to optimize it are discussed in Kung.<sup>10</sup>

Processor arrays exhibit the following characteristics:

- The latency ( $L$ ) is the schedule time interval between the first and the last computation of a single problem instance (also called block).

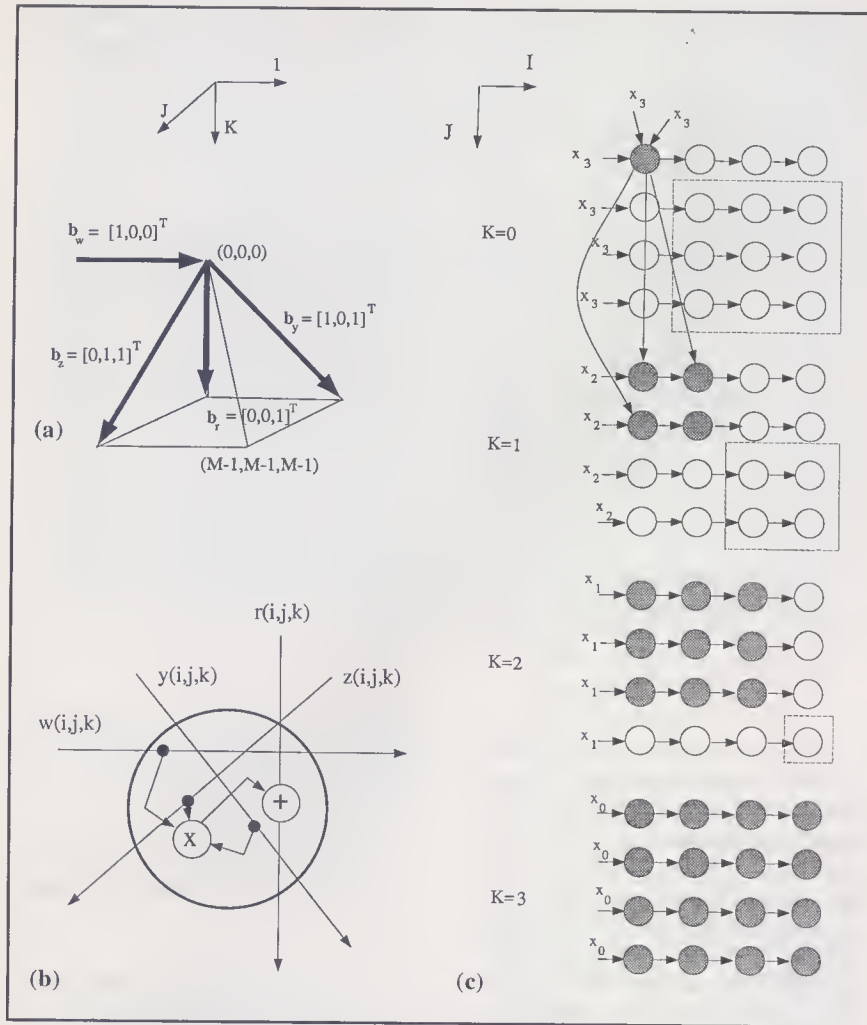


Figure 1. The skeleton of the localized dependency graph for calculation of the third-order cumulants (a); the  $(i, j, k)$  DG node (b); and the DG planes ( $M = 4$ ) (c). The dark nodes are active. The  $w$  dependencies only are shown, except in the node  $(0, 0, 0)$  for clarity.

- The pipelining period ( $\alpha$ ) is the schedule time interval between two successive computations in a processor. It is directly related to the processor's utilization.

- The block pipelining period ( $\beta$ ) is the schedule time difference between execution initiation of two successive problem instances. It is related to the overall execution time of a DSP application with multiple blocks.

In the CMM, both the node assignment (also called the projection operation) and the scheduling are chosen to be linear transformations. Given a localized DG, the designer might select many permissible (projection, schedule) combinations. Each pair leads to a valid SFG array option.

## Bispectrum estimation from the third-order moments.

Given  $\{x_k\}$ , a real, discrete, zero-mean stationary process, its bispectrum is defined as

$$B(w_1, w_2) = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} R(m, n) \exp \{-j(w_1 m + w_2 n)\}$$

where  $R(m, n)$  is its third-order moment; that is,  $R(m, n) = E\{x_k x_{k+m} x_{k+n}\}$ . Many algorithms for bispectrum estimation are discussed in Nikias and Raghuveer's tutorial paper.<sup>3</sup> We use a conventional algo-

rithm that directly employs the incoming data and the definition. Let  $\{x_1, x_2, \dots, x_N\}$  be a given data set. Then, its bispectrum can be estimated as follows:

(1) Segment the data into  $K$  blocks of  $M$  samples each; that is,  $N = KM$ . Assuming that  $\{x^{(i)}(k), k = 0, 1, \dots, M-1\}$  are the data of the  $i$ th block after subtracting the block's mean value from every sample, obtain an estimate of the third-moments (cumulants) sequence,

$$r^{(i)}(m, n) = \frac{1}{M} \sum_{l=s_1}^{s_2} x_l^i x_{l+m}^i x_{l+n}^i \quad (1)$$

where  $i = 1, 2, \dots, K$ ,  $s_1 = \max(0, -m, -n)$  and  $s_2 = \min(M-1, M-1-m, M-1-n)$ .

(2) Average  $r^{(i)}(m, n)$  over all the blocks; that is,  $\hat{R}_{m,n} = 1/K \sum_{i=1}^K r^{(i)}(m, n)$ .

(3) Generate the bispectrum estimates:

$$\hat{B}_{IN}(w_1, w_2) = \sum_{m=-L}^L \sum_{n=-L}^L \hat{R}(m, n) W(m, n) \cdot \exp \{-j(w_1 m + w_2 n)\} \quad (2)$$

where  $L < M-1$  and  $W(m, n)$  is a two-dimensional smoothing window function.

It has become apparent to many researchers that the above algorithm is very time consuming and that a real-time implementation is beyond the capabilities of today's signal uniprocessors. Hence, parallel processing is required. Computation of the bispectrum estimates based on Equation (2) corresponds to the multiplication of matrix  $\hat{R}$  with a known weight matrix. Numerous parallel architectures for matrix multiplication can be found in the literature.<sup>10</sup> Therefore, the challenge is to propose an architecture that can optimally compute the estimates of the third-order moments for multiple data blocks in a pipelined fashion. In addition, such an architecture should accommodate the final matrix multiplication step.

## Systolic array design for the third-order moments

Given a block of  $M$  samples  $\{x_0, \dots, x_{M-1}\}$ , the estimates of the third-order moments (cumulants) are defined as:

$$r(i,j) = \frac{1}{M} \sum_{k=0}^s x_k x_{k+i} x_{k+j}$$

where  $i, j = 0, 1, \dots, M-1$  and  $s = \min \{M-i-1, M-j-1\}$ .

A simple recursive algorithm to perform the above equation is given by

$$\begin{aligned} &\text{For } i, j \text{ from } 0 \text{ to } M-1 \text{ do} \\ &\quad \text{For } k \text{ from } 0 \text{ to } s \text{ do} \\ &\quad \quad r_{ij}^{(k)} = r_{ij}^{(k-1)} + x_k x_{i+k} x_{j+k} \end{aligned} \quad (3)$$

with final values  $R_{ij} = r_{ij}^{(s)}$ . Equation (3) is in SAF. However, it is not localized because of the global dependency of all  $r_{ij}^{(k)}$  on the public externally provided data tokens  $x_k$ ,  $x_{i+k}$  and  $x_{j+k}$ . To transform algorithm (3) to an LRA and avoid broadcasting, transmittant variables are introduced. To draw an analogy, the  $w$ ,  $y$ ,  $z$  transmittant variables can be thought as "horses" that are loaded once with some public data token and then carry the public data token step by step throughout the algorithm's recursions. Specifically, the  $w$ 's carry public token  $x_c$  (where  $c = 0, 1, \dots, M-1$ ) along direction  $i$ , the  $y$ 's carry  $x_c$  along the contour  $i+k=c$ , and the  $z$ 's carry  $x_c$  along the contour  $j+k=c$ . Thus, we end up with the following LRA:

$$\begin{aligned} &\text{For } i, j \text{ from } 0 \text{ to } M-1 \text{ do} \\ &\quad \text{For } k \text{ from } 0 \text{ to } s \text{ do} \\ &\quad \quad w(i, j, k) \leftarrow w(i-1, j, k) \\ &\quad \quad y(i, j, k) \leftarrow y(i-1, j, k+1) \\ &\quad \quad z(i, j, k) \leftarrow z(i, j-1, k+1) \\ &\quad \quad r(i, j, k) \leftarrow r(i, j, k-1) \\ &\quad \quad \quad + w(i, j, k) y(i, j, k) z(i, j, k) \end{aligned}$$

where  $w(-1, j, k) = x_k, \forall j, y(-1, j, k+1) = x_k \forall j, z(i, -1, k+1) = x_i \forall i$  and  $r(i, j, -1) = 0 \forall i, j$ . The final outputs are  $R_{ij} = r(i, j, s)$ . We point out here that both the transmittant variables  $w, y, z$  and the partial results  $r$  might change direction of propagation and still yield the same final results. Therefore, many equivalent LRA algorithms are possible for the same problem. Actually, this gives the array designer a lot of flexibility in the optimization attempt relative to a variety of conflicting criteria. However, at the same time it creates a large number of possible solutions to be carefully evaluated, motivating the need for a useful automation tool.

In our case, we find it advantageous to reverse the propagation direction of the partial results  $r$  so that a minimal latency schedule can be obtained. By changing the  $(i, j, k)$  coordinate system to  $(I, J, K)$ , ( $I = i, J = j, K = M-k-1$ ) we get the LRA described below:

$$\begin{aligned} &\text{For } I, J \text{ from } 0 \text{ to } M-1 \text{ do} \\ &\quad \text{For } K \text{ from } 0 \text{ to } s \text{ do} \\ &\quad \quad w(I, J, K) \leftarrow w(I-1, J, K) \\ &\quad \quad y(I, J, K) \leftarrow y(I-1, J, K-1) \\ &\quad \quad z(I, J, K) \leftarrow z(I, J-1, K-1) \\ &\quad \quad r(I, J, K) \leftarrow r(I, J, K-1) \\ &\quad \quad \quad + w(I, J, K) y(I, J, K) z(I, J, K) \end{aligned}$$

Figure 1a shows the skeleton of the pyramid-like shaped localized DG. The dependence arcs are described by  $\vec{b}_w = [1, 0, 0]^T$ ,  $\vec{b}_y = [1, 0, 1]^T$ ,  $\vec{b}_z = [0, 1, 1]^T$  and  $\vec{b}_r = [0, 0, 1]^T$ . Figure 1c shows the vertical DG plane cross sections (when  $M=4$ ) and the associated  $w$  dependencies. The dark nodes are active, each representing a multiply-accumulate computation (Mac) with non-zero operands in general. Such a computa-

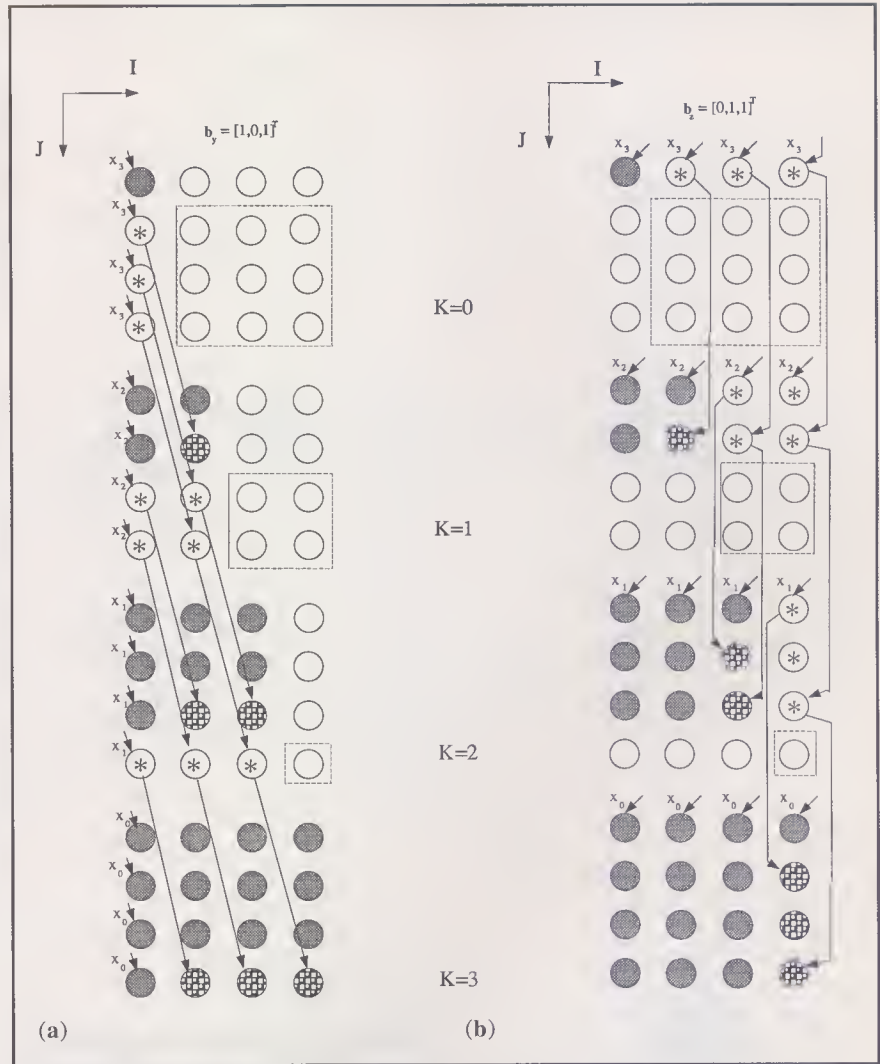


Figure 2. Dependencies of the  $y$  (a) and  $z$  (b) variables. The checker-filled nodes receive input from the star nodes. No internal input is required.

tion is considered as nontrivial. For reasons we explain later, the pyramid-like DG has been embedded in a 3D cubic framework. The  $y$  and  $z$  dependencies are shown in Figures 2a and 2b.

To derive the SFG, we choose a projection direction  $\vec{d}$  and a schedule vector  $\vec{s}$ . The projection direction  $\vec{d}$  also determines the processor basis  $\mathbf{P}$  (since  $\mathbf{P} \perp \vec{d}$ ). Every node  $\mathbf{u} = (I, J)$  of the DG is mapped to a node  $\mathbf{v} = \mathbf{P}^T \mathbf{u}$  of the SFG and the processor array. Not all schedule vectors are permissible. For a systolic array design,  $\vec{s}$  is permissible if both the following conditions are satisfied, for any DG dependency arc  $\vec{b}$ ,

$$\vec{s}^T \vec{b} > 0 \text{ and } \vec{s}^T \vec{d} > 0$$

Let  $\mathbf{u}_1$  and  $\mathbf{u}_2$  be two DG nodes and  $\vec{b} = \mathbf{u}_1$

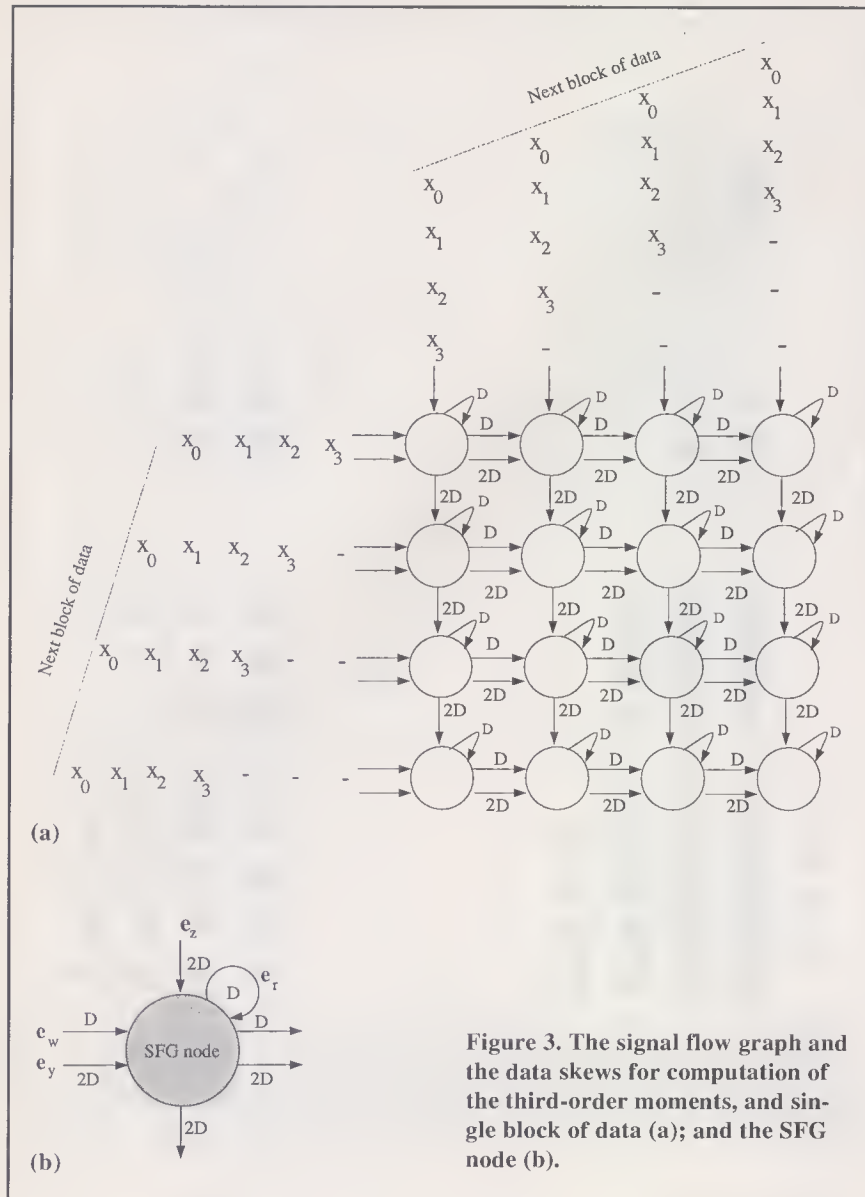


Figure 3. The signal flow graph and the data skews for computation of the third-order moments, and single block of data (a); and the SFG node (b).

—  $\mathbf{u}_2$  a direct dependency vector between them. Then,  $\vec{s}^T \vec{b} = \vec{s}^T \mathbf{u}_1 - \vec{s}^T \mathbf{u}_2 = t_{u_1} - t_{u_2}$  and the first condition says that there should be at least one time delay between successive computations assigned to the same SFG node. The second condition means that the equitemporal hyperplanes should not be parallel to the projection direction  $\vec{d}$ .

Our optimization objectives are to find a  $(\vec{d}, \vec{s})$  combination that achieves minimal latency ( $L$ ), minimal pipelining period ( $\alpha$ ) to guarantee maximum processors utilization and minimal block pipelining period ( $\beta$ ), since the bispectrum estimation involves the calculation of the third-order cumulants of multiple successive data

blocks. If we choose  $\vec{d} = [0, 0, 1]^T$  by solving an integer programming problem, we find that the minimal latency schedule is  $\vec{s} = [1, 1, 1]^T$ . Indeed, the latency is  $L = 3M - 2$  (minimal) and the pipelining period  $\alpha = \vec{s}^T \vec{d} = 1$  (minimal) in this case. The resulting time invariant SFG appears in Figure 3. It has been derived from a totally regular DG, and hence the PE control is very simple.

An essential constraint related to the VLSI implementation is that all the data inputs must occur at the boundary PEs only. A major disadvantage of our array is that it requires direct input to nonboundary PEs, as you can see by carefully examining the DG planes of Figure 2. The dark DG

nodes are either mapped to an interior array node but do not need external input, or require an input but are mapped to a boundary array node. These nodes do not cause any problems.

However, the checkers-filled nodes do cause trouble. They all require external input for either variable  $y$  or  $z$  and are mapped to an interior SFG node. Keeping the same schedule and projection, we have to modify the DG so that the resulting array will require input from the boundary PEs only. To do so, we utilize the star nodes that do not correspond to any useful computation. They pass the necessary input tokens to the checkers-filled nodes.

Realizing that the input  $y$  and  $z$  of a star node are not both nonzero is important, since the node would otherwise be dark belonging to the original DG. In fact, by checking the same DG node locations in Figures 2a and 2b, we can verify that a star node in the one corresponds to a white (trivial) node in the other. Therefore, star nodes do not contribute anything to the partial result  $r(I, J, K)$ . Furthermore, the need for internal input in the array can be eliminated at no cost to latency or extra control.

To analytically verify the correctness of the SFG, you can use the chosen projection and schedule to construct the space-time transformation  $T$ .

$$T = \begin{bmatrix} \vec{s}^T \\ \vec{p}^T \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \dots & \dots & \dots \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

A DG node  $\mathbf{u} = (I, J, K)$  is then mapped to an array node  $\mathbf{v}$  and assigned for execution at SFG location  $(I, J)$  during period  $I + J + K$ . This becomes apparent from

$$\mathbf{v} = T \cdot \begin{bmatrix} I \\ J \\ K \end{bmatrix} = \begin{bmatrix} I+J+K \\ \dots \\ I \\ J \end{bmatrix}$$

The arcs  $\vec{b}$  of the DG are mapped to edges  $e$  of the SFG with edge delays  $D(\vec{e})$

$$\begin{bmatrix} D(\vec{e}_w) & D(\vec{e}_y) & D(\vec{e}_z) & D(\vec{e}_r) \\ \dots & \dots & \dots & \dots \\ \vec{e}_w & \vec{e}_y & \vec{e}_z & \vec{e}_r \end{bmatrix} = T \cdot \begin{bmatrix} \vec{b}_w & \vec{b}_y & \vec{b}_z & \vec{b}_r \end{bmatrix} = \begin{bmatrix} 1 & 2 & 2 & 1 \\ \dots & \dots & \dots & \dots \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}$$

**The optimized array design.** In the resulting array, the PE utilization is not uniform, but it decays from 1 to  $1/M$  as the

indices  $I, J$  increase. To maximize the array utilization, we can use the otherwise idle PEs for the computation of the third-order moments of another data block concurrently.

Moving the analysis one level of abstraction higher, we see in the DGs of Figures 1 and 2 that many nodes correspond to trivial computations. For instance, node  $(3, 3, 2)$  in Figure 1 is a white node; that is, it does not contribute anything to the generation of a useful result. Thus, it does not belong to the active DG nodes. The other levels  $K = 1, 0$  also contain similar nodes (all enclosed in a square box of dashed lines).

Figure 2 also shows the symmetry between the "useful" DG nodes and the white ones. At  $K = 0$ , there is a  $3 \times 3$  square of trivial nodes (boxed), at  $K = 2$  a  $2 \times 2$  square, and so on. Since trivial nodes are translated to free PE time "slots"; we can push PE utilization to the maximum (unity) by embedding into these DG positions another equivalent DG, corresponding to the cumulants computation of a new block of data.

Geometrically, the formation of the new DG can be achieved by rotating the original one over the origin and translating it so that node  $(0, 0, 0)$  becomes node  $(3, 3, 3)$  in the embedding. The "useless" node positions of the previous DG (single block) are now filled with the active nodes of the new DG. An undesirable side effect of the rotation is the reversal of the dependency arcs direction, relative to the single block case, making scheduling of the combined DG impossible. However, because of the associativity of the Mac operation, reversing them once more to create a two-blocks-combined DG with the same dependencies orientation as in the single block case does not present a problem. Figure 4 depicts the final result where the two DGs coexist in a perfect manner; that is, they do not share nodes, and all their dependency arcs have common directions.

Before examining the two-blocks-combined DG more closely, let us elaborate on how the new DG works and how it can be mapped to a processor array. Figures 4a and 5a show that the top ( $K = 0$ ) level requires loading for the transmittant variable  $w$  from the left side (boundary in the array), but also it requires loading of the  $y$ 's and  $z$ 's directly to the internal DG nodes. Stated another way, broadcasting is required for loading the  $y$ 's and  $z$ 's at the top level before the computation can start.

Broadcasting can be avoided by localizing the DG of Figure 5a to obtain the one of

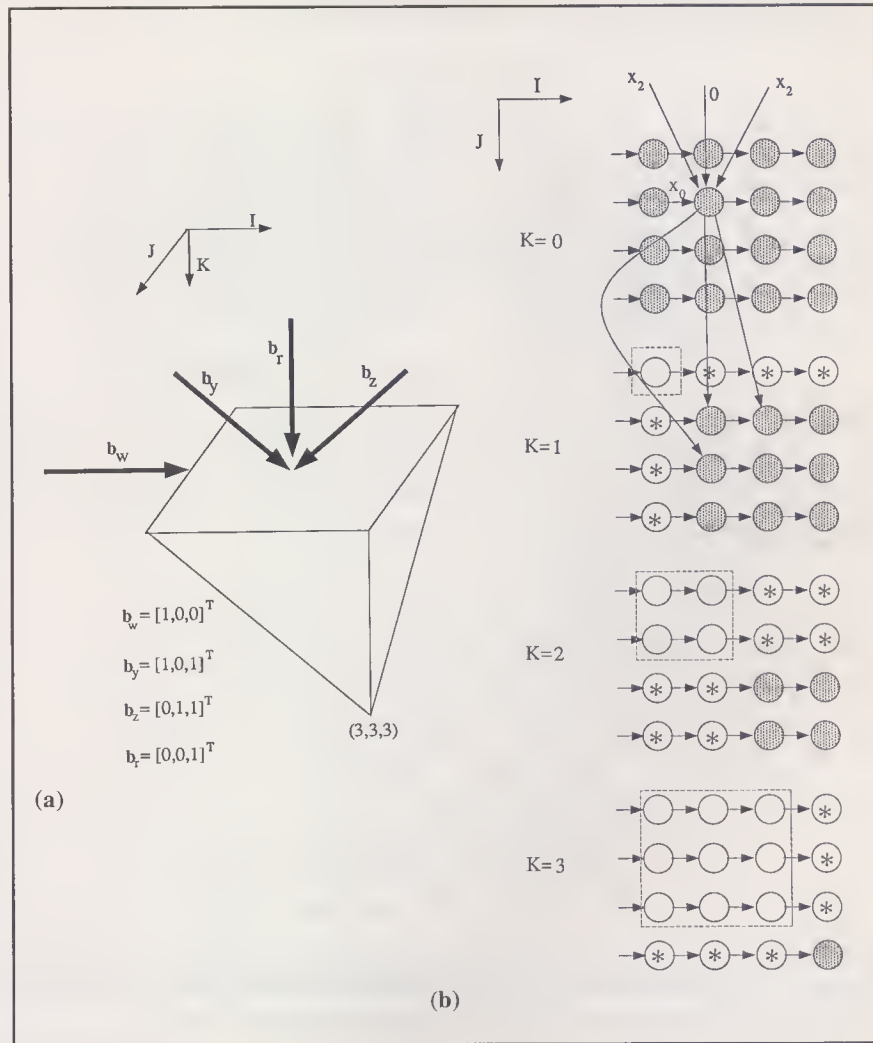


**Figure 4.** The skeleton of the new pyramid-like DG (a); and the embedding of the new DG into the original index space (b). Only the  $w$  dependencies are shown, except for node  $(1, 1, 0)$  for clarity. Dark nodes are active; all others correspond to the single block case (see Figure 2).

Figure 5b. Now, the  $y$ 's are propagating along  $J$  and the  $z$ 's along the  $I$  direction one step at a time. Assuming that every DG node becomes an SFG node, the resulting loading phase SFG is shown in Figure 5c. For example, the first instant PE  $(0, 0)$  computes the quantity  $x_0 x_3^2$  and propagates the  $y$  variable (carrying token  $x_3$ ) to the PE  $(0, 1)$  and the  $z$  variable (token  $x_3$ ) to PE  $(1, 0)$ . These  $y, z$  will be used at the next schedule time at PEs  $(0, 1)$  and  $(1, 0)$ , respectively. This way, all the internal DG nodes of level  $K = 0$  receive their input tokens exactly when they need them without broadcasting.

Figure 6 shows the vertical cross sections of the two-blocks-combined DG. Two

different fillings (and superscripts) have been used to indicate the active nodes of the two merged DGs. The star nodes are "spent" for data propagation to the internal nodes as explained before (see Figure 2).

We observe that multiplexing the  $w$ 's of the two blocks is necessary because they are loaded from the same boundary side and they might need to pass through nodes of a different block to reach their consumption destination. The  $y$  and  $z$  data streams are confined in their associated block so there is no need for multiplexing. Keeping the same projection and schedule vectors to preserve the optimal properties of the single block SFG (see Figure 3), we end up with the SFG of Figure 7a, which is nothing

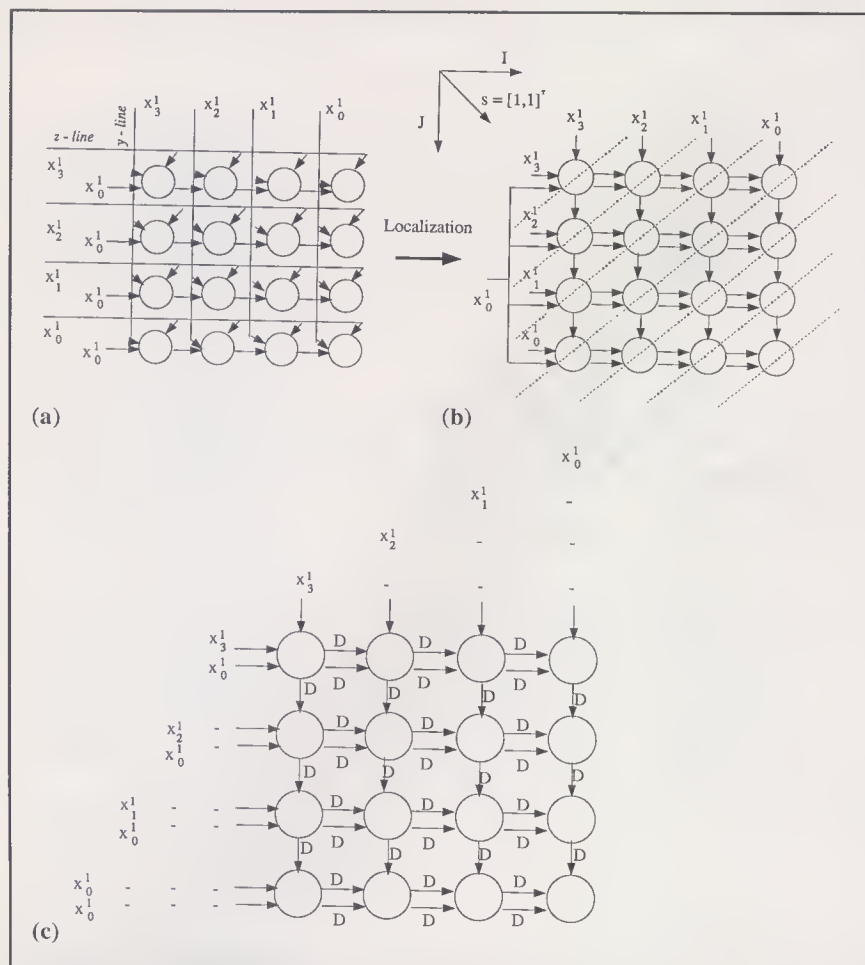


Figure 5. The nonlocalized DG for the loading phase (upper plane,  $K = 0$ ) (a); the localized DG (b); and the resulting SFG and data skews (c).

ing more than the union of the SFGs of Figure 3 (single block) and Figure 5c (loading phase), as expected.

Figure 7b shows the structure of the array node, which contains six registers for storage of the variables  $w^1$ ,  $w^2$ ,  $y$ ,  $z$ ,  $r^1$ , and  $r^2$ ; six multiplexers for the inputs; a decoder; and a Mac unit. For every set of two successive data blocks and at every time instant, each PE can perform one of the following functions:

- (1) first, compute the partial result  $r_{i,j}^1$  of block No. 1 (loading phase);
- (2) then, contribute to the partial result  $r_{i,j}^i$  of either block No. 1 or block No. 2 ( $i = 1$  or  $2$ ).

Simultaneously with the computation, the PE transmits  $w$ ,  $y$ ,  $z$  variables to its near neighbors with appropriate delays as derived by the CMM.

So that every PE can recognize which

function to perform at a specific time instant, it must have a status register to indicate its position ( $I, J$ ) and a local counter of  $M + 1$  stages. Based on the contents of these registers, three control bits ( $c_1$ ,  $c_2$ ,  $c_3$ ) are generated that are enough to control the I/O multiplexing.

Bit  $c_1$  determines the block upon which the PE is currently operating. Bit  $c_2$  indicates the current phase (that is, normal loading), and bit  $c_3$  indicates whether the PE operates on a star node of the DG. If so, the  $w^2$  latch must be reset to zero to guarantee that there will be no computation involved, thus destroying the desired result. Among all these controls, only the local counter depends on the block size. The control strategy is very simple and can be hardwired or microcoded.

Every two data blocks, a new loading phase is required but, because of the pipelining, the resulting time overhead will be only one time unit independent of the block

size  $M$ . Therefore, the optimized array exhibits a latency  $L = 3M - 1$  for the two blocks together. Also, the block pipelining period is  $M + 1$  for two blocks. Therefore, we achieved a decrease of the block latency and block pipelining period by a factor of 0.5. In addition, all PEs perform the maximum amount of useful work, having a utilization factor equal to unity uniformly across the array.

Overall, the array is optimal in terms of performance measures of interest for real-time applications with many successive data blocks. This very crucial factor is usually overlooked in special-purpose parallel processing designs. For example, an optimal pipelining period  $\alpha$  would not be sufficient in this type of application. We strived to achieve the optimal block pipelining period  $\beta$ .

Once the estimates of the third-order moments have been calculated, the same hardware can support bispectrum estimation. This fact can be verified by observing that the definition formula (1) degenerates to matrix-matrix multiplication after appropriate initialization. We are not including the complete details of the initialization in this article due to limitations of available space and because the procedure is straightforward.

**R**eal-time performance of biomedical signal image processing applications demands the transition from uniprocessor to multiprocessor architectures for CBMSs. Systematic vertically integrated design methodologies should be used to reduce the design turnaround time of such parallel processing systems. Using such methodologies before making a commitment to a final design would facilitate exploration of different architectural solutions and effectively address validation, performance, and fault tolerance concerns.

As discussed in this article, the canonical mapping methodology can elucidate critical trade-offs in the design of a special-purpose VLSI processor array for higher order spectral analysis, a relatively new digital signal/image processing discipline that has recently demonstrated a great deal of potential in many biomedical applications.

The special-purpose processor array for the computation of the third-order moments (cumulants) we proposed constitute the first and most important step in HOS analysis. Our array is optimal in terms of latency and block pipelining, two very crucial factors in environments where

continuous real-time flow of data blocks is expected.

The design has been carried out systematically, as opposed to the ad hoc ways usually employed in problems of similar complexity. The correctness has been proved analytically, demonstrating the feasibility of formal verification—a property absolutely essential in CBMSs.

A description of the PE's function and structure can be written in a hardware description language (such as VHDL) and interfaced with VLSI synthesis libraries to reduce the overall custom design turnaround time.

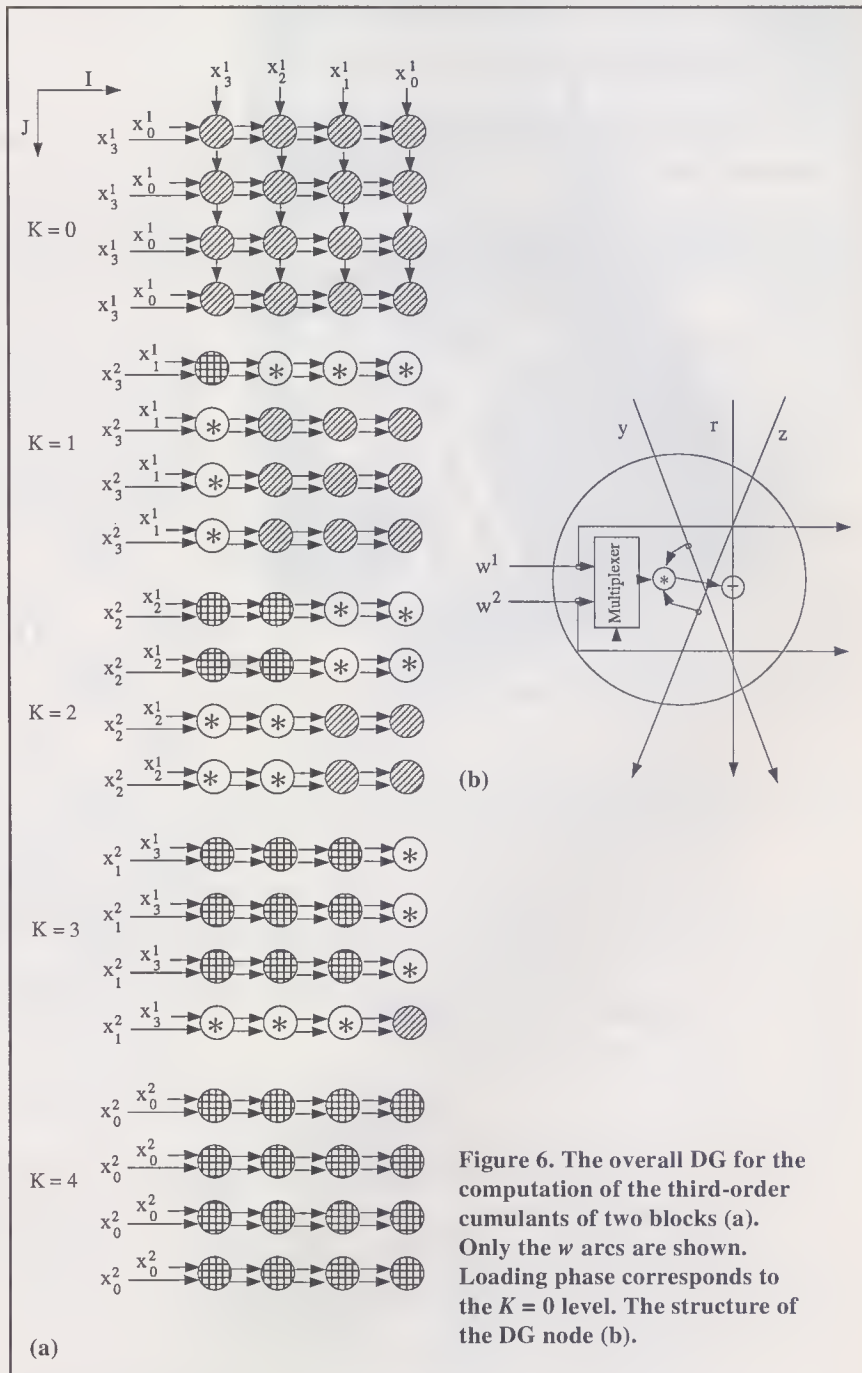
Because of these emerging CAD capabilities, we expect the use of parallel processing to extend HOS applicability to real-time signal image processing soon. Such an advancement will create the potential for new biomedical applications for diagnostic, imaging, and life-support systems, and will contribute to clinical assessment in many medical fields. ■

## Acknowledgment

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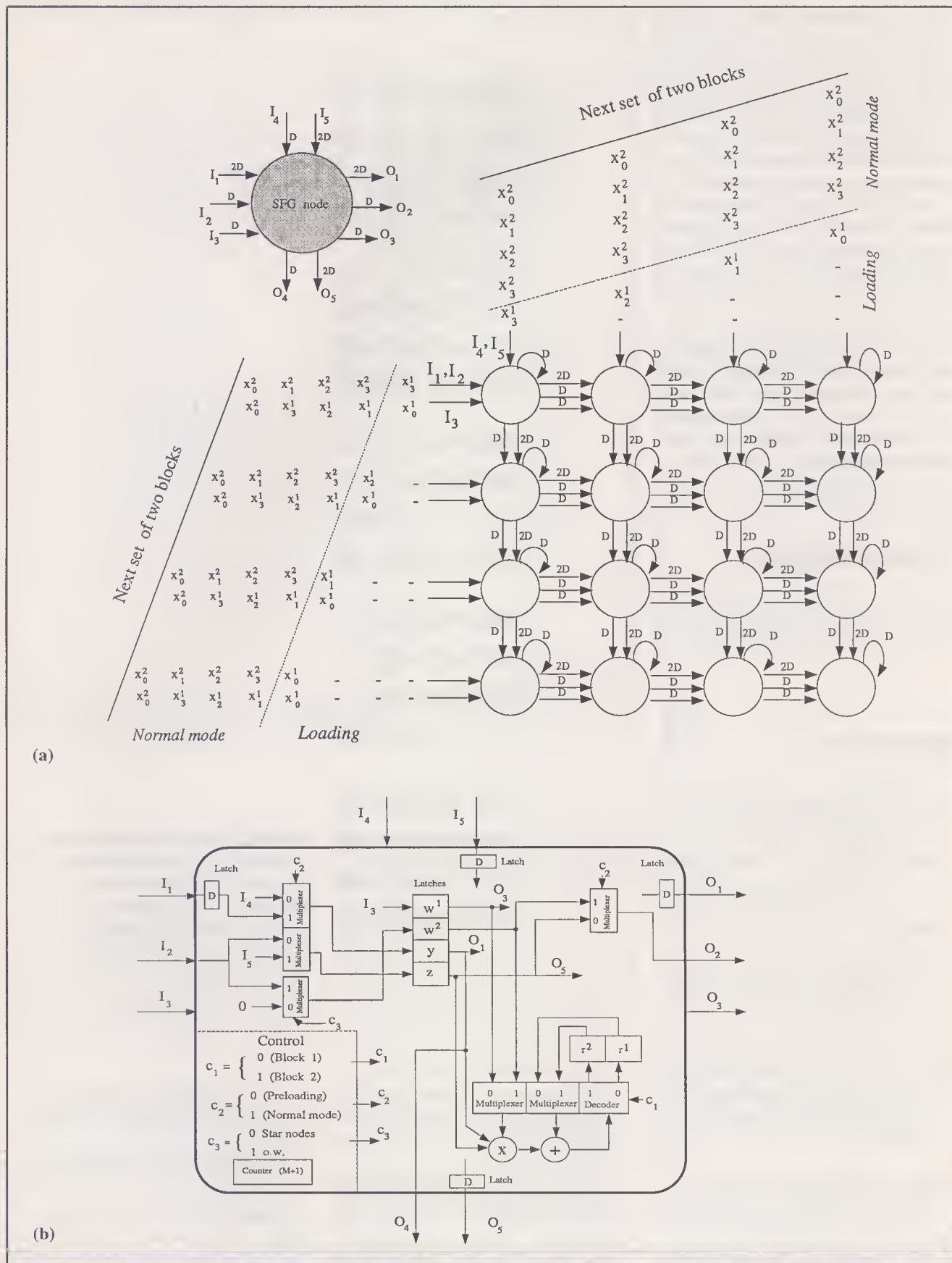


Figure 7. The resulting SFG for computation of the third-order moments of two data block (a); and the array node's internal structure (b).



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# Neuronet

## A Distributed Real-Time System for Monitoring Neurophysiologic Function in the Medical Environment

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**T**his article focuses on a specific medical application at the Center for Clinical Neurophysiology at the University of Pittsburgh. The application is served by Neuronet, a large software package integrated with 80 computer workstations and instrumentation. It provides both off-line and real-time capabilities. The application addresses many problems that must be solved for computer-based systems that function in the medical environment. The application's real-time components can be life critical; the administrative support elements interact in a complex fashion with the life-critical ones.

The center provides diagnostic and intraoperative monitoring services throughout the university health center. These services assess patients' central and peripheral nervous system function using electrophysiological and vascular measurements. The numerous staff-level clinicians who participate in the service are academicians with individual research interests and styles in administering procedures. Thus, Neuronet has been configured to provide a host of readily accessible and continually expanding tools for running clinical neurophysiology studies.

### System overview

The environment in a tertiary health care center such as the University of Pittsburgh



**Neuronet provides immediate access to real-time life-critical data being acquired at multiple sites across the health center and allows one neurophysiologist to simultaneously monitor multiple surgical procedures.**

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medical center requires provision of service without delay or inconvenience to the referring physician at all times. Although it is expensive to provide enough equipment to cover peak times, the primary difficulty is in providing competent staff neurophysiologists to oversee multiple simultaneous procedures throughout the complex.

The university's health center encompasses seven hospitals. At any time, a dozen or more procedures may simultaneously

require a neurophysiologist's supervision. To enhance the observational ability of the staff neurophysiologist on call, a variety of remote capabilities were incorporated in Neuronet, including manual remote display, automatic remote display, and manual remote-message passing.

The sequence of events that occurs to initiate, provide, and support clinical neurophysiology services is as follows:

- (1) The physician orders a diagnostic study or intraoperative monitoring.
- (2) The study is scheduled with the patient.
- (3) Staff and equipment resources are committed and positioned at the designated time and place.
- (4) The patient is brought to a staffed diagnostic laboratory, or staff and equipment are brought to the operating room at the appropriate time.
- (5) The study is obtained.
- (6) A report is generated, and a note is entered in the chart.
- (7) The data are archived.
- (8) A bill is generated and dispatched.

The network of person-to-person transactions that enables this sequence is shown in Figure 1. This sequence of events is facilitated by conceptualizing the basis of the service as a local area network (LAN). The overall system is run on this network in a distributed environment. The file system

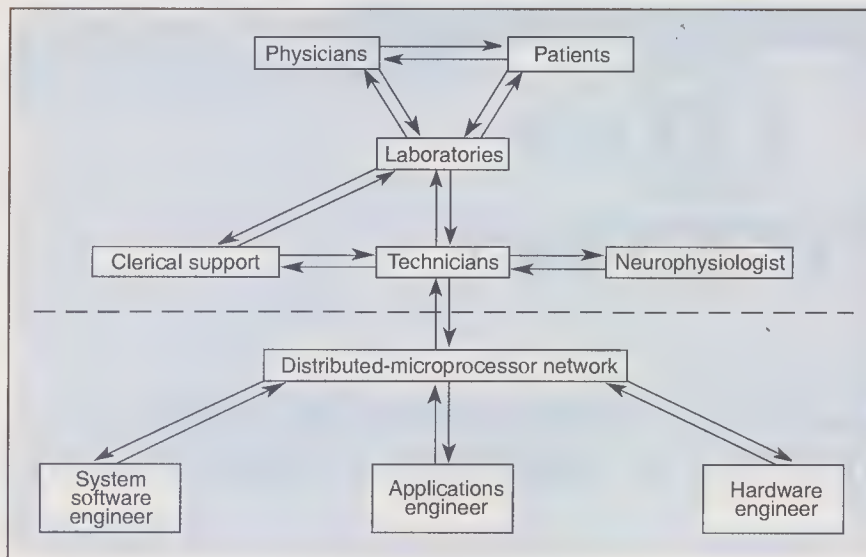


Figure 1. Summary of transactions in the neurophysiology group. The distributed-microprocessor network and its supporting personnel (below the dashed line) are transparent to the user community (above the dashed line).

is decentralized, the database is distributed, and servers for diskless nodes are placed in pairs to provide redundancy in case of hardware failure. The network has a 10-megabit-per-second Ethernet backbone (IEEE 802.3) with proprietary 12-megabit-per-second token-passing-ring subnetworks from Hewlett-Packard/Apollo. Figure 2 shows the currently operating network of computer systems in the health center.

Attached to the LAN are both fixed and portable computers, each associated with appropriate electronics for providing services for which that equipment rack will be used. This network of machines provides the following key capabilities:

- scheduling,
- applying stimuli with simultaneous data acquisition,
- computer processing for arithmetic data manipulation and display,
- archiving data,

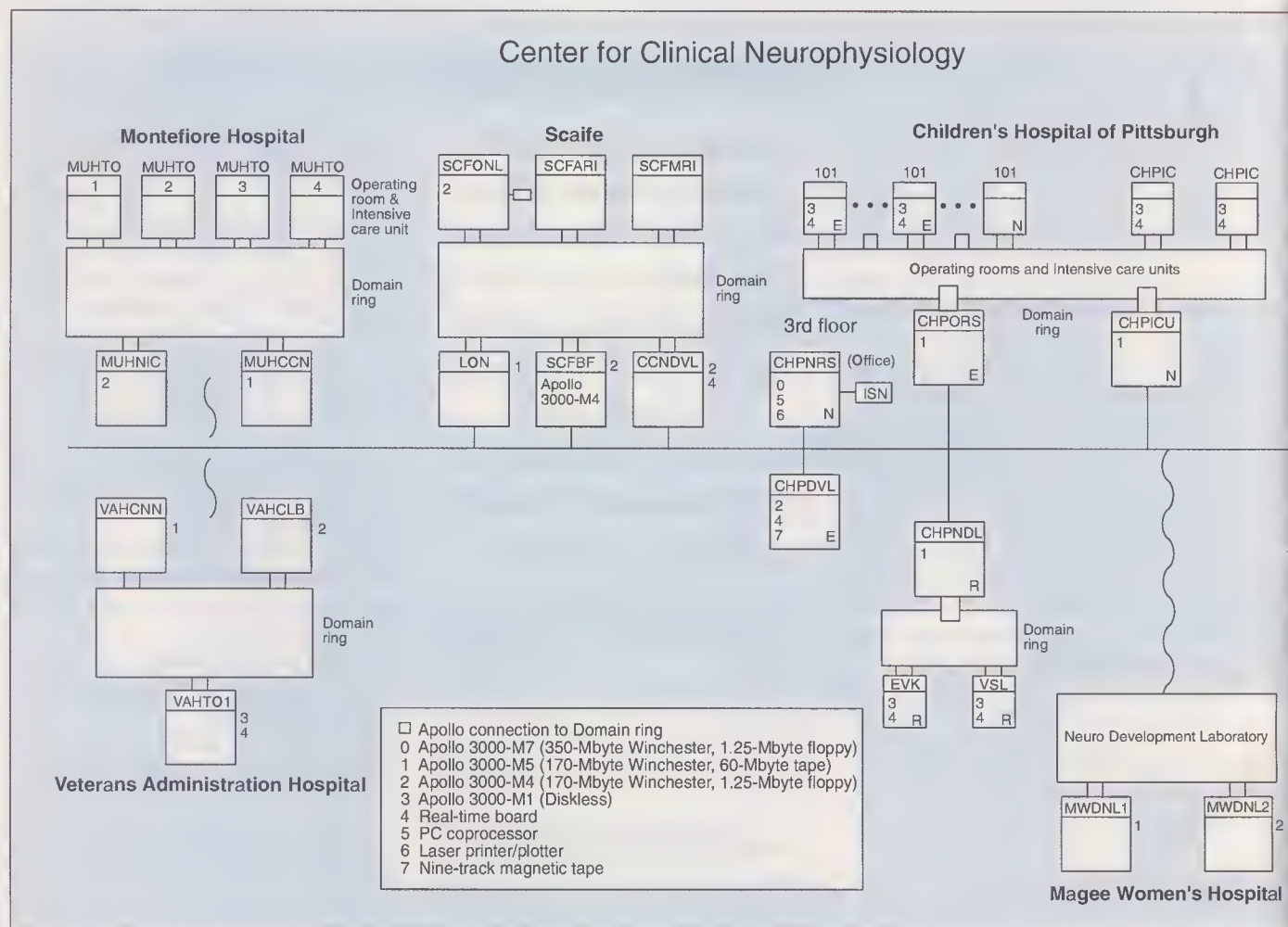


Figure 2. Current Neuronet configuration. The horizontal line spanning the figure represents the Ethernet backbone. Each token-passing ring is attached to the Ethernet through a gateway. The connections to Montefiore and the Oakland

- managing resources, and
- billing.

Neuronet applications span a wide spectrum of real-time performance requirements. In the operating room, evoked-potential acquisition, processing, and immediate display can be life critical. For other functions, brief delays are tolerable, for example, for database interactions while scheduling a patient over the telephone. Still other functions can be performed off line, for example, archiving data, managing resources, billing, and generating reports. In addition to time considerations in designing the system, reliability in the face of regular software and hardware upgrades is a key system requirement.

Hardware upgradeability was one of the primary requirements that led to the use of a LAN. Software upgradeability is maintained by conforming to the spiral life-cycle model<sup>1</sup> for software development with

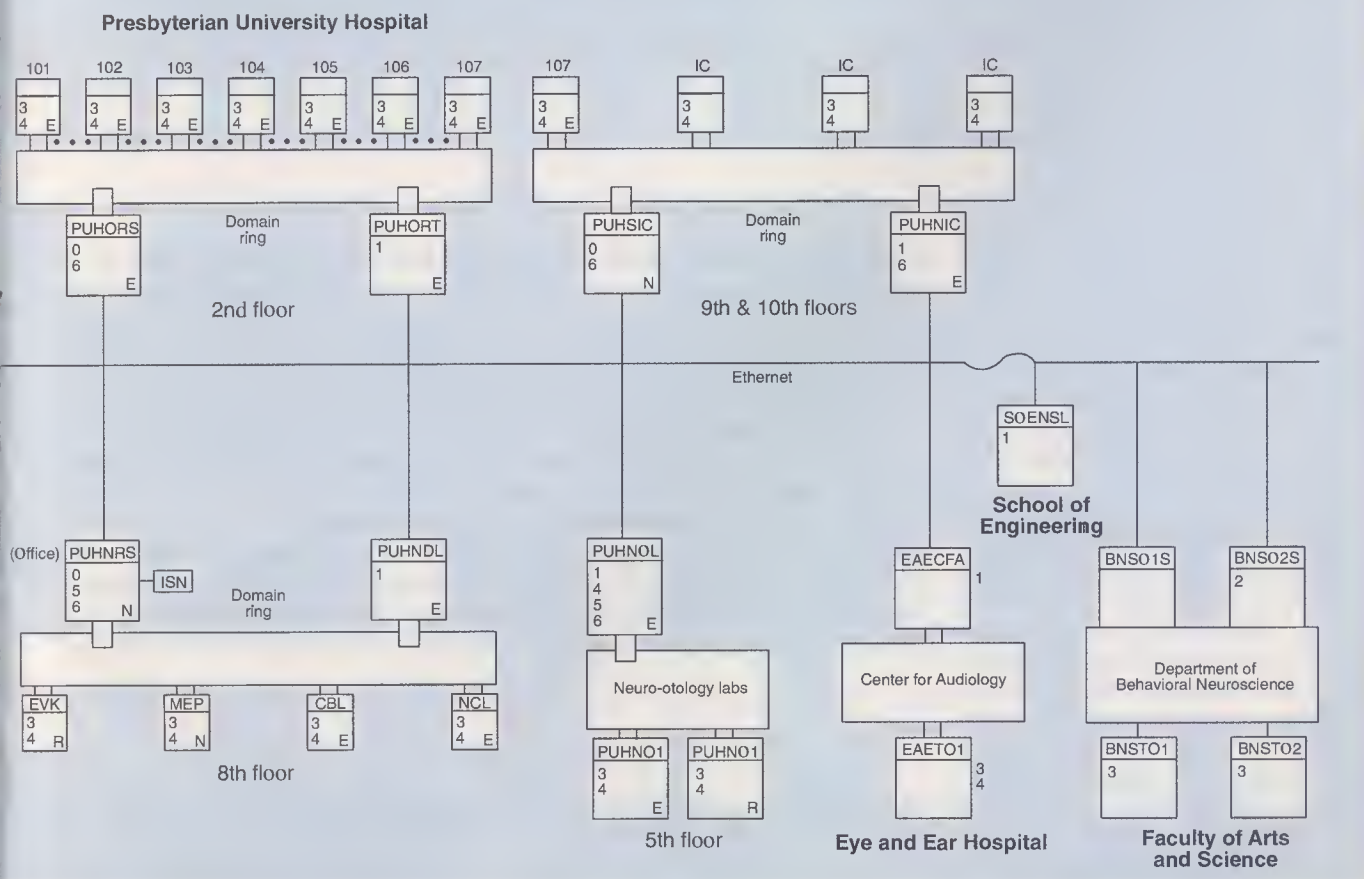
a sequence of more and more extensively exercised installations provided to the user.

For scheduling, managing resources, generating reports, billing, and eventual direct interfacing to the main hospital information system, a Codasyl (Conference on Data Systems Languages) database was chosen and integrated with the software package. The real-time applications include a wide and constantly expanding set of signal processing capabilities. In addition to local processing, a sequence of innovations has been introduced that enables remote real-time data display. Data can be acquired at one location on the network and displayed simultaneously in many other locations, both across the network and over voice-quality telephone lines. A significant portion of the program development effort has focused on the development of an effective and well-organized human interface that is used consistently throughout the software package.

The practice of clinical neurophysiology includes a wide range of diagnostic and monitoring techniques.<sup>2,3</sup> Diagnostic techniques include neuroelectric measurements from muscle, the scalp, vascular measurements, and others. A neurophysiological measure provides information about nervous system function, distinguishing it from anatomical techniques that provide information about structure — for example, computed tomography, also known as CT.

The intraoperative neurophysiological techniques are primarily based on electrical measures, although the direct dependence of nervous system function on blood supply calls for blood-flow measurements in some cases. The electrical measures of interest have relatively short time constants, on the order of 1-10 milliseconds. However, the electrical environment in the operating room is noisy, and there is background electrical activity produced by the

## Center for System Neuroscience



Veterans Administration hospitals are via voice-quality phone lines. The backbone is attached to the Internet through the University of Pittsburgh's gateway.

central nervous system. Therefore, most neuroelectric measures taken in the operating room are collected over many seconds and arithmetically processed to produce interpretable information. This processing includes averaging, digital filtering, and estimation and background noise removal for single trials.<sup>4</sup>

## Case example

The aorta, which supplies blood to most of the body, including the brain and spinal cord, is abnormally narrowed in some children. Repair usually requires cross clamping — that is, clamping the vessel on either side of the narrowed area, removing the narrowed area, and rejoining the severed vessel. In a small percentage of coarctation repairs, about 1 in 300, the spinal cord does not tolerate the loss of blood supply that occurs with an aortic cross clamp. To prevent spinal cord injury, cord function can be monitored by repeatedly applying electrical stimuli to sensory nerves in the lower limbs and recording the response of the central nervous system at the scalp. If the neural pathways that carry this evoked response — including the spinal cord — are compromised, a change in the response will be detected.

The evoked response at the scalp is about 5 microvolts and appears on a background of normal brain activity of 20 to 100 microvolts. To extract this small signal from the background and electrical noise in the operating room, it is necessary to present many stimuli, typically 70 to 120, and process the response to each stimulus to produce an interpretable response. At a stimulus rate of 3 to 5 hertz, an interpretable evoked response is obtained every 20 to 35 seconds, providing relatively rapid feedback to the surgeon regarding spinal cord function.

Figure 3 shows sample results from a repeat coarctation repair in a 12-year-old. As indicated by the arrows in Figure 3a, responses from the beginning of the case until the moment of beginning of aortic cross-clamp application were consistent. As soon as the artery was clamped, the waveform lost its consistency (traces 86 to 89). The surgeon immediately removed the clamp, and the responses returned. To maintain blood flow, the surgeon then placed the vessels that supply the spinal cord on a pump that bypassed the aortic cross clamp. Figure 3b shows that the response remained stable following bypass placement, even with the aortic cross clamp.

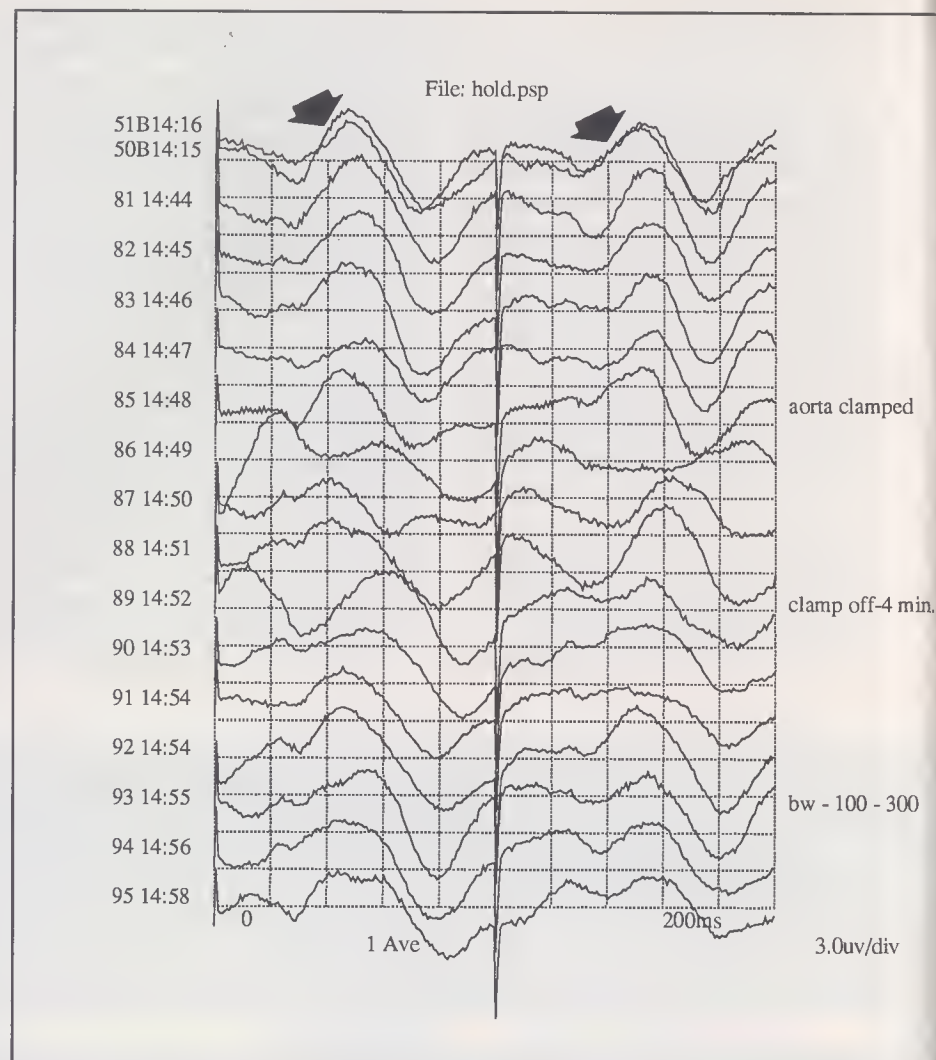
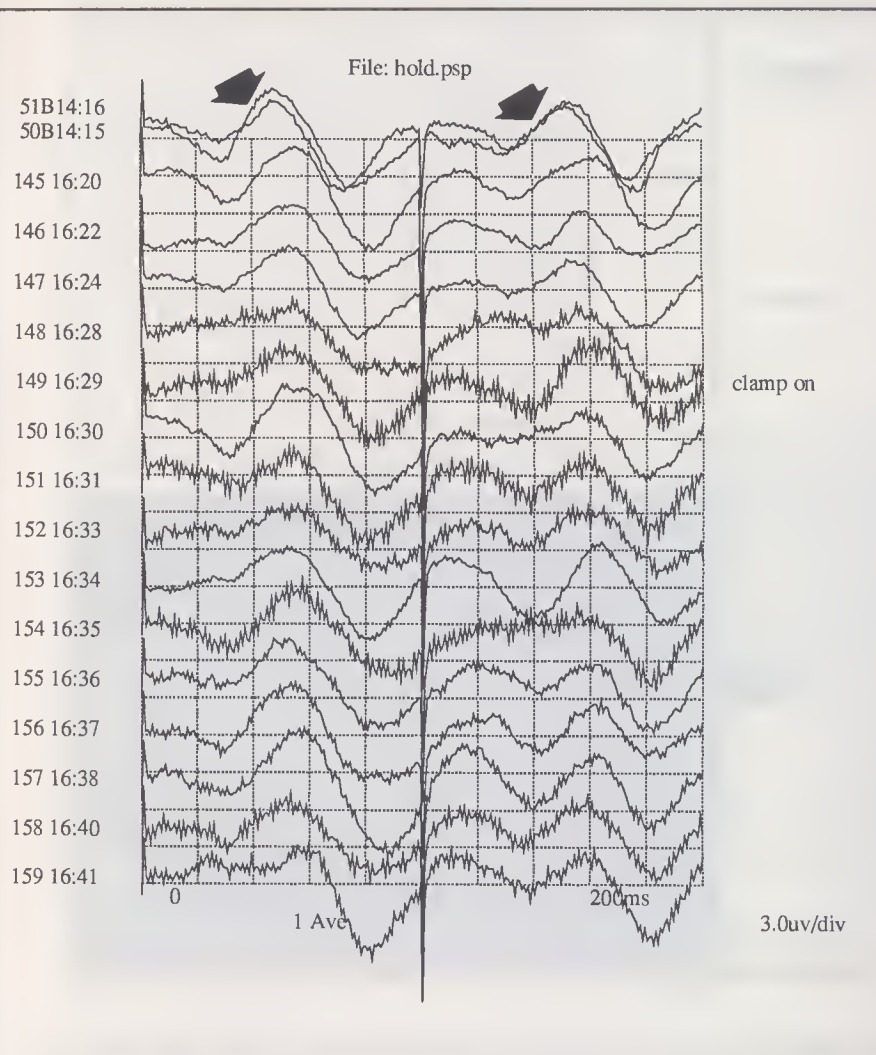


**Figure 3.** Case example. Shown are two intraoperative monitoring displays of peroneal nerve responses to twin-pulse stimulation. These displays are available during the case both in the operating room and at any node attached to the network. Responses were obtained during critical moments in an aortic coarctation repair procedure in a 12-year-old girl. Each stimulus consisted of a shock to the left peroneal nerve followed 100 milliseconds later by a shock to the right peroneal nerve. Stimulus artifacts are prominent at the 0 and 100 milliseconds marks in each trace. A total of 128 responses were averaged for each trace. The recording electrodes were located at International 10/20 System placements Pz (active) and Fz (reference). Positive voltage is represented upward. Time and voltage scaling are shown at the bottom. The number of each trace and the clock time at which it was obtained are shown at the left. Note that traces proceed in temporal sequence from the top of the figure to the bottom. Comments entered by the technician during the case are shown at the right. Two superimposed baseline

## Remote capabilities

A coarctation repair typically lasts three to five hours, with responses obtained about every 45 seconds. Since there is significant

spinal cord compromise due to aortic cross clamping in only 1 out of 300 cases, the intraoperative monitoring, although time critical, is a vigilance task. There are other cases in which the contribution is more immediate and occurs with much higher



traces obtained early in the case are shown at the top with the cortical evoked response indicated by arrows.

Trace 86 (part a) was obtained during the first minute following aortic cross clamp. Note the disintegration of this waveform compared with those that preceded it. The clamp was removed during the course of trace 87. The trace showed some variability for several minutes due to dramatic blood-pressure changes following aortic unclamping.

Traces 149 through 159 (part b) were obtained following aortic cross clamp with a circulatory-assist bypass pump in operation. There was no significant change compared with preceding traces other than what could be accounted for by blood-pressure changes. The bypass pump was turned on at trace 148 as indicated by the increased noise level.

probability. For example, in reconstructive hip surgery, the incidence of sciatic-nerve palsy is approximately 1 out of 10 cases. In surgery for large acoustic neuromas, the likelihood of facial-nerve palsy and/or hearing loss is higher still. In those

cases, monitoring is more efficient in terms of the number of cases for which a contribution is made, although the seriousness of many of the potential complications is considerably less. The value of multiple observers in a vigilance task, in addition to

the personnel resource considerations, has stimulated the development of a set of remote display capabilities. Although the need for these capabilities has been recognized, there are few reports available and limited development of such capabilities to date.<sup>5-7</sup>

All remote capabilities are implemented through files that can be accessed from anywhere on the network. Although this approach is slightly slower than one in which messages are passed directly from processor to processor, it is more conservative of critical system resources: CPU time, network time, and memory. This can be seen by examining a remote display for evoked-potential data that is being acquired in the operating room. The computer that acquires and processes the data for local display is a diskless workstation sitting in an instrumentation rack. Diskless machines are used for several reasons:

- (1) The instrumentation racks are wheeled from room to room. Using diskless machines avoids the danger of mechanical damage to a Winchester disk.
- (2) They are less expensive.
- (3) Using disks in fixed machines assures that all disk space will be accessible at all times.
- (4) The machines that run in the operating room are relieved of the CPU and bus loading associated with disk services.

The instrumentation rack workstations perform the following functions:

- data acquisition and stimulus presentation;
- artifact rejection via several algorithms, including a primary clipping algorithm;
- signal averaging;
- digital filtering, when selected;
- plus/minus averaging, when selected (this is a noise estimation procedure);
- initiation of file storage of completed evoked responses (completion is determined when a set number of nonartifact-contaminated trials are averaged);
- initiation of ongoing disk storage of the partially completed evoked response to a special place in the file every three seconds;
- constant update and display of the ongoing partially completed evoked response; and
- constant update and display of the completed evoked responses in waterfall form, compressed-spectral form, or density-spectral form.

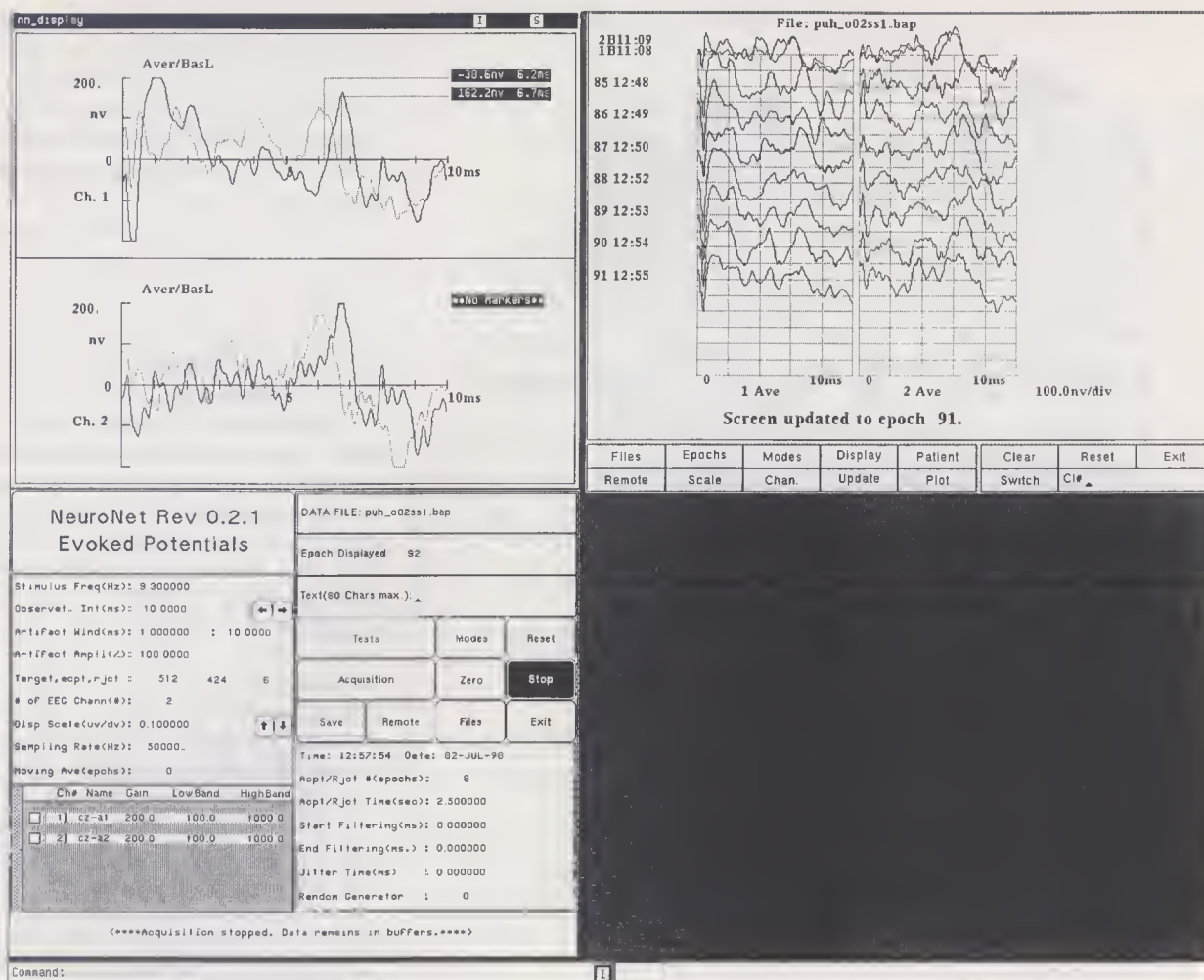


**Figure 4.** Typical operating room display during evoked-response monitoring. The upper left panel shows the current, partially completed, evoked response (solid line) superimposed on a baseline evoked response from the beginning of the case (dotted line). Note that the current response is delayed by 0.5 milliseconds compared with the baseline. The lower left panel shows all the parameters and controls for acquiring evoked responses. Note that the stimulus frequency is 9.3 hertz, the observation interval is 10 milliseconds, etc. These are typical parameters for acquiring brain-stem, auditory evoked responses as shown here. The upper right panel shows a waterfall display of evoked responses acquired over the past several minutes. This window is similar to those shown in Figure 3.

Figure 4 shows the display from an instrumentation rack workstation that acquires and displays evoked-response data. The server node — from which the diskless node is booted — performs all data-storage functions. If a remote node elsewhere on the network requests data from the file, the server handles the request, thus relieving the diskless node from further computational or other burdens. The file can be opened for read-only access by multiple nodes across the network, or even across the Internet using FTP (file-transfer protocol). The file is opened by a process running on a node elsewhere on the LAN from

which a user wishes to view the data acquired in the operating room; the data is read and displayed as the remote observer wishes. The remote observer can also access the ongoing, partially completed, evoked response.

Automatic remote viewing is accomplished by a shell script. Data from intraoperative monitoring and diagnostic studies are stored in a specific subdirectory on each server. The shell script searches this subdirectory continuously on all network servers. Any time it finds a file that has been updated in the last 10 minutes, it brings up a copy of the remote display

process with all display parameters automatically set to appropriately display the data. A window is created on the screen of the automatic remote monitoring node that continuously updates the display as new data is saved by the diskless acquisition node in the operating room or diagnostic laboratory. If a file goes more than 10 minutes out of date — that is, the case or diagnostic study is over — the shell script terminates the remote display process and clears the screen space for another display process. Thus, a dynamically changing picture of all the studies across the network is maintained automatically and continu-

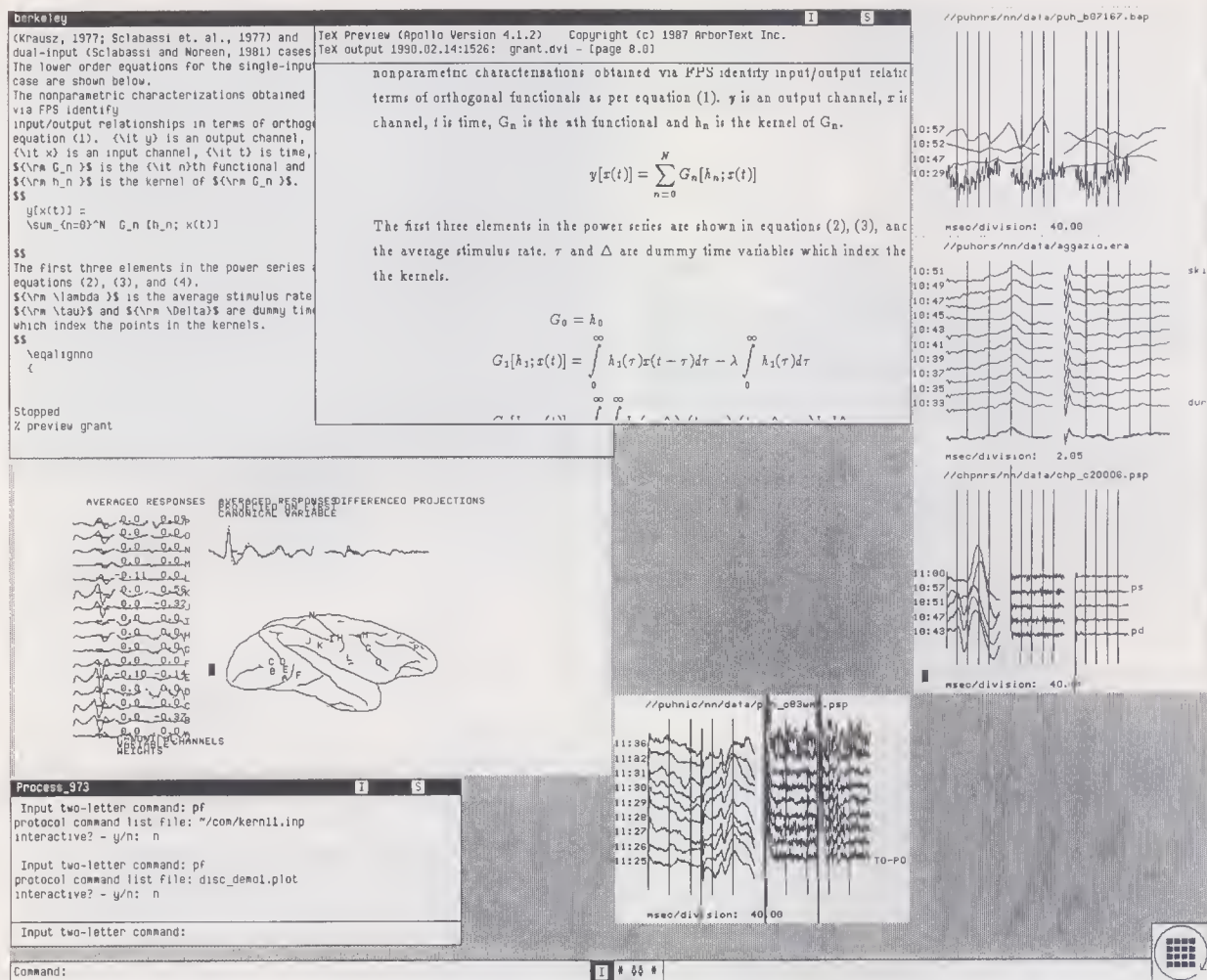


**Figure 5.** Typical remote monitoring display. This figure shows a display obtainable from anywhere on the network. The small box at the lower right corner contains a process that is automatically and continuously searching for active operating room or diagnostic studies. The four small windows containing waterfall displays were spawned by this process and display one ongoing diagnostic study (upper right corner) and three operating room cases. The two text windows at the top show a manuscript in preparation. The figure in the center was produced using the process shown in the lower left window.

ously by this automatic remote display function. From any node on the network, a single neurophysiologist can oversee all the clinical activity in the health center for which he is responsible, while at the same time maintaining other activities. A typical display from a remote monitoring node is shown in Figure 5.

Remote message passing is carried out through the remote display processes and can be initiated from anywhere on the network. Messages can be sent in both directions and appear along with a bell that sounds to alert the user. In this way, the staff neurophysiologist can communicate

quickly (one to two seconds) and at will with any operating room and with multiple technicians.

These remote capabilities constitute partial surveillance of events that occur in the operating room and diagnostic laboratory. To extend these functions, we plan to add a private phone system and a local cable TV network controlled through the same mouse-driven button. Extending the neurophysiological data transmission functions to the multimedia ones that are under development<sup>8</sup> will significantly improve a single neurophysiologist's ability to effectively monitor multiple simultaneous procedures.

## Signal processing

In each acquisition and display routine, there are multiple hooks provided for signal-processing capabilities. In most programs, the user can access these capabilities through mouse-driven push-button menus. New signal-processing schemes are added by adding subroutines to the code. The user invokes these schemes by clicking on new lines that appear in the menus. In display routines, whenever signal-processing functions are invoked, the raw signal is also displayed. This assists in recog-

The figure displays three overlapping screenshots of a medical database interface. The top-left window shows a 'PATIENT' form with fields for Patient ID (123-456-789), Birthdate (6/18/48), Last name (Doe), First (John), M.I. (N), Sex (Male), Race, Phone, Address, Refer MD, Diagnosis, and Exam. It includes a 'Data Entry Pages' sidebar with checkboxes for Patient, Phone, Address, Refer MD, and Diagnosis. The top-right window shows an 'EXAM' form with fields for Exam No., Exam Location, Patient Location, Month (6), Day (29), Year (1990), Test time (60), Type (OR), and Exam Time. It includes a 'Data Entry Pages' sidebar with checkboxes for Patient, EXAM, Modality, Medication, and Instruction. The bottom-left window shows a 'Diagnosis List' and 'Patient's Diagnosis' section, with a 'Data Entry Pages' sidebar. The bottom-right window shows a 'Procedure' section with a list of procedures and a 'Data Entry Pages' sidebar. All windows have an 'EXIT' button at the top and 'SAVE', 'REPLACE', 'DELETE', and 'DONE' buttons at the bottom.

Figure 6. Typical demographics display. Three copies of the demographics database routine are shown to demonstrate program features; in normal use, only one copy is used by one user. The three windows represent three records in the top two layers of the data structure shown in Figure 7. The upper left window shows the menu of items used to enter or display a patient. The lower left window shows the menu of items used to enter or display the patient's diagnoses. The lower right window shows the menu of items used to enter or display an exam. Note that only one record can be displayed at a time, but that the parent and offspring records of the displayed records are shown in the lower left panel. This panel can be used at any time to transit the data structure. The upper left panel contains one key item from each parent and grandparent record.

dition of any distortion that may be introduced by the signal-processing techniques. It also facilitates the recognition of the signal features for whose enhancement the signal-processing technique has been applied.

An arbitrary digital filter can be applied to any signal under study. Digital filters are stored in files that can be selected from a menu. A new filter can be defined by invoking the function for that purpose. Additional signal-processing capabilities that have been included in one or more of the acquisition or analysis routines include frequency analysis using Fourier trans-

form or discrete Wigner Ville time-frequency representation, notch filtering using regression, plus/minus averaging on alternative epochs to provide a measure of background noise, and others. A variety of other techniques are being studied and developed in prototype routines. In addition to signal processing, several different display modalities are provided, depending on the program. For example, for spontaneous brain activity, a user can select raw display, compressed-spectral array, density-spectral array, fast Fourier transform averaging, or time-frequency density spectra.

## User interface

The user interface was designed to be easy to learn and use and to respond rapidly. In most cases, it is a mouse-driven interface. Parameters are set by clicking on arrows that raise or lower them. When a parameter is set to a nonstandard value, the user types in the desired value. All mouse buttons are used in a standard way across all programs. Clicking the left button enables a selection. Clicking the right button obtains a short help message for the item selected.

For prototype program development, much work was done with a terminal interface. This assisted in rapid conversion of programs that were developed on main-frame computers with terminal access only. More recently, prototyping with the mouse-driven interface has been used because the programming tool for this interface, Domain Dialogue, allows rapid development of prototype software. An additional advantage is that using a mouse-driven button interface from the beginning provides a first cut at the final user interface; thus, the final software version is one step closer to completion.

User-interface development was an important motivating factor in the use of an evolving prototype software model. This model has enabled numerous revisions of the interface in response to input from a wide variety of users around the health center.

User interface examples are shown in Figures 4 and 6. Figure 4 shows the interfaces for the evoked-response acquisition and waterfall-display programs. Figure 6 shows the interface for the D3M-based program to enter and access demographic information (see **Database**). Figure 4 shows that critical real-time functions, such as starting and stopping the acquisition and saving an epoch, are large and easily identified. Additional functions are presented in other buttons. For example, the user can select a baseline epoch from an arbitrary file anywhere on the network, a variety of digital-filtering techniques, numerous data-display options, etc.

## Database

This package required the following functions of a database management system integrated with real-time acquisition and processing:

- storing demographic information,
- documenting and tracking real-time data, and
- storing secondary variables defined during data scoring as part of the effort to produce a report.

The secondary variables include peak heights and latencies from evoked potentials, a variety of blood-pressure and velocity measurements from trans-cranial Doppler, and English-language comments and interpretations that can be integrated as part of a report.

The database management system that

was chosen was bundled with the Hewlett-Packard/Apollo workstation software, D3M. D3M is a Codasyl database with a number of special features that make it attractive for development.

D3M is distributed; access to it is provided by server processes running on nodes all over the network. Many users can simultaneously access a particular database at any time. Any collisions — attempts to change the same record by multiple users at the same time — are adjudicated by the server processes. Furthermore, a database can be divided among many files existing on separate disks across the network. This provides considerable latitude in constructing redundant records for robust operation in case of disk failure.

The system software provides access to D3M via calls from a variety of programming languages, including Fortran, C, and

Pascal. In addition to this access, all calls that involve transactions to D3M contain English-language statements that describe what is to be done. Thus, each call that includes a transaction is documented in the call itself.

The typical Codasyl data structure shown in Figure 7 was developed to support these functions. This data structure provides tremendous flexibility for storing data in an organized fashion while providing rapid access through a hash table. It is integrated with other software components to enable multiple access at multiple levels for different functions.

Access to the upper layers is via the user interface shown in Figure 6 or, more commonly, through the real-time acquisition program and scoring programs. For example, the computer can sense the amplifier gain and filter settings during evoked re-

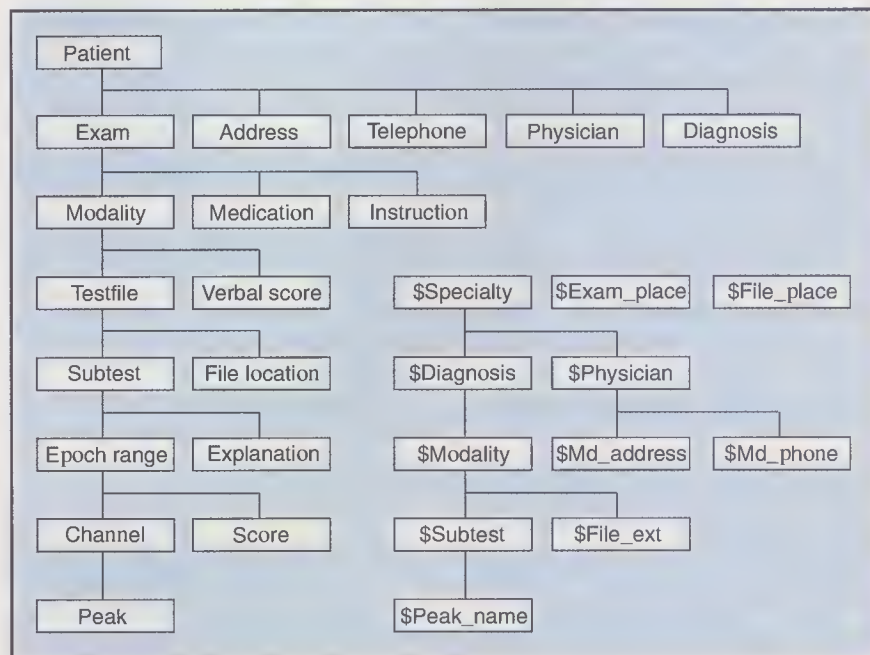


**Figure 7.** The Codasyl data structure used in Neuronet. Each element in the diagram is called a record and is composed of one or more items of information. Records are owned by records above them in the diagram. There can be multiple versions of a particular kind of record attached to a single record above. For example, each patient can have multiple exams, physicians, etc.; each exam can have multiple modalities, etc. The items in the records in the upper two layers of the structure on the left contain demographic information. These layers are primarily accessed through the user interface shown in Figure 6. The lower layers are for storing waveforms or other scores, amplifier settings, and other parameters used for specific tests. The records on the right whose names begin with a dollar sign contain both site-specific items (for example, names of physicians) and generally useful information (for example, common interpretation phrases). These items can be changed only by the system administrator.

sponse and electroencephalogram studies. Once a study is done, these values are set in the database for the permanent record. These parameters can be changed from one epoch (complete averaged evoked response) to the next, and the new values will also be stored. Conversely, previously stored parameters can be used to automatically set up a study. Parameters that can be controlled through the database include amplifier gain and bandpass, acquisition rate, stimulus rate, and others.

## Reliability and upgradeability

The software package was originally developed on LSI-11 (Digital Equipment Corporation) computers attached to an Ethernet backbone.<sup>9</sup> The software was then ported to a workstation environment. At the same time, the Ethernet backbone was extended with token-passing-ring subnetworks.<sup>10</sup> Development continued in this multiprocess programming environment to the form described here. To carry development forward efficiently and dependably, while maintaining the functionality of the computer network on a day-to-day basis, the spiral life-cycle model has been used.<sup>1</sup>

Each software unit is treated as an evolving prototype. New functions are developed as stand-alone routines or as subroutines that are used in a variety of ways. However, new routines are always backed up by the tried-and-tested routines that form the service's bread-and-butter functions. As new functions are developed and tested for their functionality and user interface, a professional applications programmer incorporates them in the standard package and further tests them in the development laboratory.

A sequence of four complete software installations is maintained at all times on the network. If a previously unrecognized catastrophic fault is present in a recent software revision, a user can rapidly retreat to a previous, better tested version. This retreat is accomplished by logging out and then logging in to the desired environment through a different account name. A user logging in to a particular environment is automatically and transparently pointed to the software revision corresponding to that account name through a symbolic link. This link is "soft" by virtue of a logical environmental variable included as part of the link name. This use of soft links enables rapid installation and change of the

software of a specific account by simply changing the environmental variable. Although this approach is cruder and slower than the *N*-version approach to fault tolerance,<sup>11</sup> it is functionally equivalent for this purpose.

The four installations with their functions are listed below:

(1) Betaneuro. Only one version of Betaneuro exists on the network. Betaneuro is the most recently revised software version and is used under close programmer and neurophysiologist supervision to test new functions for utility, dependability, etc.

(2) Newneuro. Once Betaneuro is tested by the neurophysiologists and deemed useful for the operating room without close technical supervision, Betaneuro is installed on every server in the network under Newneuro. The installation of this and all other versions of the software on the network provides maximal robustness in the face of potential network failure. If the Ethernet backbone goes down, or if one server goes down in an operating room ring, the software is still available on a local server to the diskless nodes running in the operating rooms.

(3) Neuro. When Newneuro is installed, the previous Newneuro is moved to Neuro. Thus, what is installed in Neuro is a version of the software that has been extensively tested — not only in the laboratory but also in the full network environment in the operating rooms and diagnostic laboratories under Newneuro. This environment, Neuro, is the one that is routinely used to support the clinical service.

(4) Oldneuro. Whenever Newneuro is moved to Neuro, Neuro is moved to Oldneuro, providing double redundancy in the software.

In general, this revision scheme is one in which modest changes are made for new revisions. Big changes are made in only one program at a time so that it is known which program must be exercised most thoroughly to validate the software revision. This development scheme has been very effective in allowing software revisions on a monthly basis. With this rapid revision schedule, the software development group can be very responsive to user needs and, at the same time, maintain high system reliability.

The present revision scheme has been in operation over the past three years, since moving to the workstation environment. It has been used continuously and without failure during monitoring of 4,000 sequen-

tial cases and 12,000 diagnostic studies. There have been several network-wide slowdowns associated with the reception of large electronic mail messages from China following the Tienamen Square incident. Although these slowdowns caused no system failures, as might be expected from a chain reaction,<sup>12</sup> they were dramatic enough to require temporary shutdown of the electronic mail capability.

**T**his article describes an extensive computer-based instrumentation system used in a large tertiary health care center. Many of the problems whose solutions are presented in the context of this specialized system are generally encountered in computer-based medical systems. Among these are expandability, robust operation in the face of potential hardware failure, regular revisions without reduction in dependability and with zero down time, real-time response, and integration with an extensive data-base management system.

The solutions that are presented are generally applicable and demonstrably effective and economical. The system has been used in its present configuration for more than three years, not only in time-insensitive applications — for example, data archival and report generation — but also in life-critical applications in multiple simultaneous procedures. ■

## Acknowledgments

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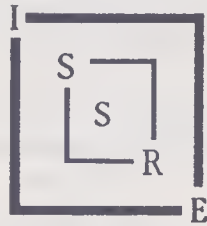
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# Using Fuzzy Sets to Diagnose Coronary Artery Stenosis

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**T**he uncertainty always present in information used to construct knowledge-based systems can be expressed in terms of Bayesian probabilities, the Dempster-Shafer theory of evidence, or fuzzy sets. This article, part of a series of studies on postexercise thallium-201 myocardial perfusion scans,<sup>1,2</sup> is concerned with the expression of uncertainty in terms of fuzzy sets. It focuses on defining a fuzzy set from training data.

Stenosis (narrowing) of the main arteries supplying the myocardium (the middle muscular layer of the heart wall) is the most common underlying cause of heart attacks. Thus, it is important to determine how severely a coronary artery blockage interferes with blood flow to the myocardium and which arteries are abnormal. In nuclear cardiology, stress thallium-201 scintigraphy is used to detect abnormalities in the distribution of blood flow to the myocardium. (Planar scintigraphy is the detection in two dimensions of a radiation source — in this case thallium-201 — in the body.) Regions of the heart with less-than-normal blood flow are said to have a perfusion defect.

The relation between the percentage of perfusion defect in a patient's scan and the severity or location of stenosis in an artery is not well defined. For example, a 50-percent perfusion defect in the basal seg-

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**Fifteen rules generated with fuzzy set theory perform as well as 68 rules specified by cardiologists in diagnosing coronary artery stenosis using thallium-201 scintigrams.**

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ment of the lateral view may indicate normal coronary arteries or an obstructed coronary artery or arteries.

Using computer techniques to help in visual interpretation of stress thallium-201 myocardial perfusion scans significantly improves the detection of coronary artery stenosis.<sup>1-5</sup> In this article, we report on the use of fuzzy sets to represent perfusion defects and to generate expert rules to help in diagnosis. We used retrospective data

collected from 91 patients who underwent both stress thallium-201 myocardial scintigraphy and coronary arteriography. We chose 64 scans at random for training and used the remaining 27 scans for testing data.

## Data collection

Data were collected from a retrospective review of 360 consecutive patients who underwent both a Bruce-protocol treadmill stress test with thallium-201 scintigraphy and coronary arteriography within 30 days. (Arteriography differs from scintigraphy in that it uses X-ray cine photography of contrast in the arteries rather than a scintillation count of radiation source.) We selected for further review patients identified from the clinical coronary arteriography report as having either normal coronary arteries or a significant obstruction of only one major coronary artery. The selected patients also had no intervening clinical event — myocardial infarction, angioplasty, coronary surgery, or change in antianginal medication — between stress testing and arteriography.

We defined a significant obstruction as equal to or greater than a 70-percent narrowing as measured visually with calipers. Normal arteries had narrowings of less

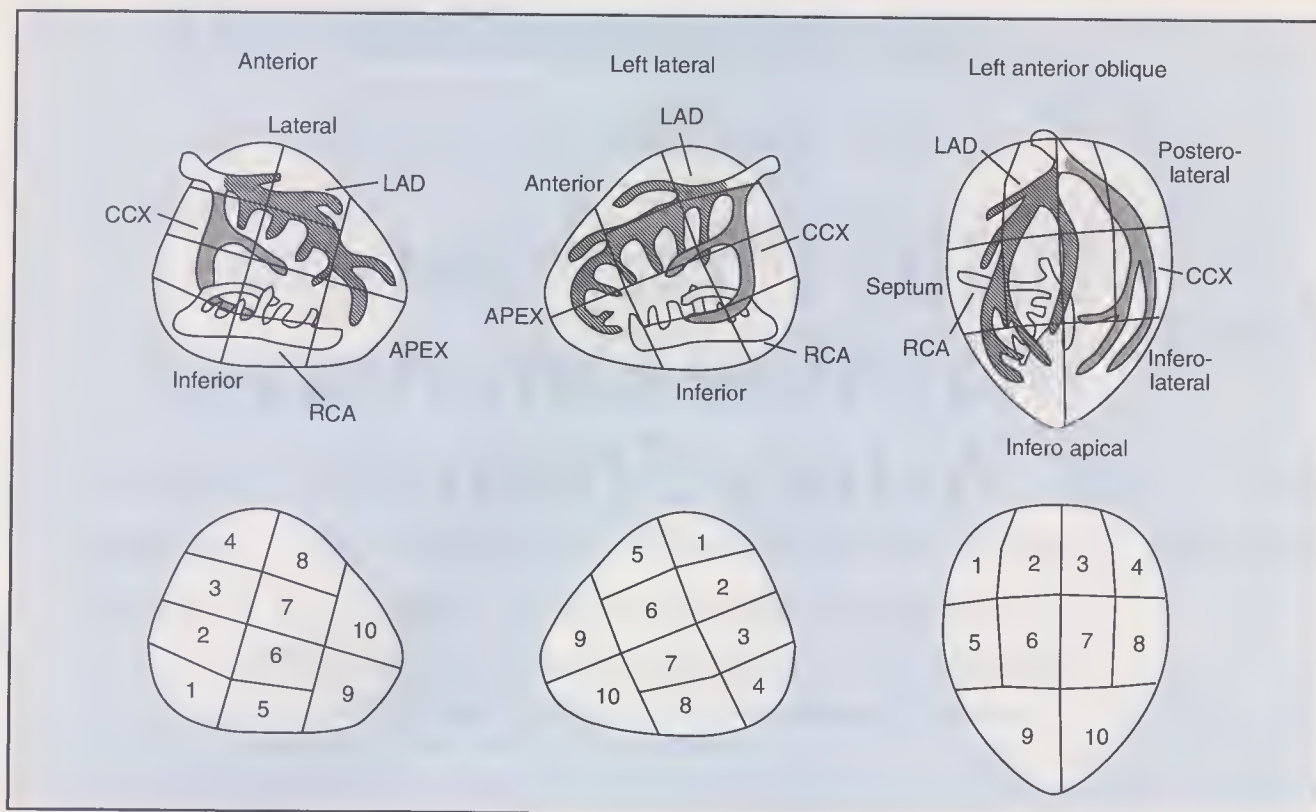


**Figure 1.** Three views of a scan and the numbering scheme for the segments of each view: CCX stands for circumflex artery, LAD for left anterior descending artery, and RCA for right coronary artery.

than 30 percent. We classified the major coronary arteries as the left anterior descending artery, right coronary artery, posterior descending artery, and the circumflex artery. For data analysis, patients having a significant stenosis upstream from the posterior descending artery were classified as having right coronary artery obstruction, regardless of whether this artery arose from the right coronary or circumflex artery.

We excluded from analysis patients having stenosis of a median ramus branch, left main coronary stenosis, and congenital anomalies of the coronary arteries affecting the expected distribution of blood flow. Fewer than 10 percent of the cases reviewed consisted of such patients.

**Scintigraphy.** Myocardial perfusion scintigraphy was performed by the standard clinical protocol. At peak exercise, thallium-201 (2 millicuries per 100 kilograms) was injected intravenously, and the patient continued exercising for one minute. Scintigraphic images were recorded from the anterior and left anterior oblique views with the patient supine, and from the left

lateral view with the patient in the right lateral decubitus position. Counts were collected with a Technicare 0.25-inch crystal portable gamma camera to a minimum of 300,000 counts or 10 minutes per view, whichever was longer.

**Scintigraphic analysis.** We processed scintigrams by comparing the normalized count ratio for each pixel at a given anatomic location with that obtained previously from a group of subjects having normal myocardial perfusion. Pixels containing count ratios that fell more than 2.5 standard deviation below normal were considered to be underperfused. Each of the three views was divided into 10 anatomic regions called segments. Figure 1 shows the numbering scheme. However, for computer analysis, the segments of all three views were numbered consecutively. Segments 1 through 10 of the left lateral view are referred to as regions 11 through 20, and segments 1 through 10 of the left anterior oblique view are referred to as regions 21 through 30.

The percentage of underperfused (as compared with normally perfused) pixels

in each region represents the magnitude of the perfusion defect for that region. Thus, 30 numbers ranging in size from 0 to 100, each representing the size of the perfusion defect in that region, were generated from each patient's scintigram.<sup>2,3</sup>

## Extracting fuzzy sets

In this article, we report on our use of fuzzy sets to handle uncertainty in the diagnosis of coronary artery stenosis. (The sidebar "Dealing with uncertainty" summarizes fuzzy sets and other ways to handle uncertainty.) The locations and extents of perfusion defects are anatomically related in a "fuzzy" way to the site of stenosis within a specific coronary artery. Therefore, we want to define fuzzy sets to represent the relationship.

We use the notion of an ordered pair consisting of two objects to define a fuzzy set. The essential property of an ordered pair  $(x, y)$  is that  $(x, y) = (z, w)$  if and only if  $x = z$  and  $y = w$ . We define a binary relation as a set whose elements are all ordered pairs. Such a set formalizes the intuitive

idea of association. We define a fuzzy set mathematically by assigning to each possible individual in the universe of discourse a value representing its grade of membership in the fuzzy set. This grade reflects the degree to which that individual is compatible with the concept represented by the fuzzy set.

We divide the training scintigraphic data into two groups, normal and "stenosed"

coronary arteries, to extract fuzzy sets representing the relation between the percentage of perfusion defect for each region and the stenosis in the coronary artery that causes it. From the training data, we obtain the relation

$$\text{"stenosed"} = \{(\text{perfusion defect}, \text{degree})\},$$

where degree denotes relative abnormality of a patient's scan.

A thresholding technique is often used to divide a continuous value into several ranges. However, if we want to use the percentage of perfusion defect to decide whether a patient's scan represents normal or stenosed arteries, it is very difficult to find appropriate threshold levels. We use fuzzy sets to circumvent this problem. The objective is to define a membership function  $\mu_i(x)$  that maps a perfusion defect of

## Dealing with uncertainty

Human knowledge often has the form of uncertain beliefs rather than crisp, indisputable facts. First-order logic represents absolute truths or absolute untruths, but it does not aid in resolving most real problems, which contain a great deal of uncertainty.

In the Bayesian method,<sup>1,2</sup> a well-known method for dealing with uncertainty, facts are modeled as hypothesis nodes of a decision tree. A number associated with each node represents the a priori probability that the hypothesis is true, when no other supporting or detracting evidence is available. A node located on the lower level of the tree represents evidence that either supports or detracts from the hypothesis by its truth or falsehood. Once the evidence is assessed, the probability of the hypothesis is recalculated.

Let  $p(H)$  be the prior probability of a hypothesis, and let  $p(H/E)$  be the posterior probability of the hypothesis, given the evidence. Then, the prior odds on  $H$  and posterior odds on  $H$  are related to the probabilities via

$$O(H) = \frac{p(H)}{p(\bar{H})}, \quad O(H/E) = \frac{p(H/E)}{p(\bar{H}/E)}$$

When the evidence is present and a measure of sufficiency,  $\lambda$ , (also called the likelihood ratio) is supplied by an expert, the posterior odds change by the factor of  $\lambda$  and are calculated as follows:

$$O(H/E) = \lambda O(H), \quad p(H/E) = \frac{O(H/E)}{1 + O(H/E)}$$

Another method of dealing with uncertainty uses the Dempster-Shafer theory of evidence, which is based on the concept of a support pair (an interval) whose endpoints are the lower and upper probability bounds. A support pair consists of two elements, the nec-

essary support, and the possible support. The necessary support,  $S$ , is the minimum support that is given to the truth value probability assignment. The possible support,  $U$ , is the maximum possible truth value probability assignment. Notation for the support pair is  $[S, U]$ .

In the Dempster-Shafer theory, a belief in a hypothesis,  $B(H)$ , is the sum of probabilities for all the subsets of  $H$ . Support pairs accommodate for the situations where the sum of the belief that a hypothesis is true and the belief that the negation of the hypothesis is also true, is less than one.

$$B(H) + B(\bar{H}) < 1$$

For  $B(H)$  and  $B(\bar{H})$  to be truth value probabilities, their sum must be equal to 1. Since this is not always the case,  $B(H)$  is called the necessary support, and the complement of  $B(H)$  is called the possible support:

$$S = B(H), \quad U = 1 - B(\bar{H})$$

Therefore, the interval,  $[S, U]$ , indicates the degree to which the evidence fails to discriminate between  $H$  and  $\bar{H}$ . That means that upon learning new evidence supporting the hypothesis, this interval can be narrowed. Having full evidence supporting the hypothesis,  $S$  becomes equal to  $U$ ; thus, the support pair reduces to a single number that is the truth value probability of hypothesis.

In this article, we concentrate on a third method — the use of fuzzy sets.<sup>5,6</sup> The basic idea in fuzzy set theory is that an element has a degree of membership in a fuzzy set. Thus, a proposition need not be simply true or false, but may be partly true. For example, the fuzzy set "tall" can have as its elements people with degrees of member-

Table A. Representation of the fuzzy set "tall."

| Height | Degree of Membership |
|--------|----------------------|
| 5'0"   | 0.00                 |
| 5'4"   | 0.08                 |
| 5'8"   | 0.24                 |
| 6'0"   | 0.50                 |
| 6'4"   | 0.76                 |
| 6'8"   | 0.92                 |
| 7'0"   | 1.00                 |

ship dependent on their height. Table A shows a possible subjective representation. A person five feet tall might have a corresponding degree of membership equal to 0, and a person seven feet tall might have a degree of membership of 1.

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Table 1. Patient data statistics (numbers indicate the region number of a whole scan).

| Number | Normal  |                   |          | Stenosed |                   |          |
|--------|---------|-------------------|----------|----------|-------------------|----------|
|        | Average | Maximum deviation | Standard | Average  | Maximum deviation | Standard |
| 1      | 0.2     | 2.0               | 0.5      | 2.8      | 27.4              | 5.0      |
| 2      | 2.0     | 8.5               | 2.3      | 11.5     | 72.5              | 16.6     |
| 3      | 0.8     | 6.1               | 1.6      | 6.7      | 64.0              | 13.1     |
| 4      | 1.7     | 7.4               | 2.3      | 7.6      | 67.4              | 16.6     |
| 5      | 0.1     | 1.2               | 0.3      | 11.2     | 60.0              | 15.7     |
| 6      | 1.0     | 5.7               | 1.6      | 27.3     | 99.1              | 28.9     |
| 7      | 0.3     | 2.4               | 0.7      | 21.4     | 100.0             | 26.6     |
| 8      | 8.2     | 27.2              | 7.9      | 26.7     | 99.1              | 31.2     |
| 9      | 0.5     | 2.8               | 1.0      | 19.6     | 88.0              | 23.4     |
| 10     | 2.8     | 18.7              | 4.6      | 32.9     | 100.0             | 29.6     |
| 11     | 15.6    | 59.7              | 15.9     | 14.9     | 93.7              | 21.0     |
| 12     | 9.9     | 53.3              | 14.5     | 9.5      | 80.5              | 15.9     |
| 13     | 6.8     | 25.2              | 8.4      | 11.3     | 96.0              | 19.3     |
| 14     | 4.0     | 18.9              | 4.8      | 20.0     | 97.0              | 21.1     |
| 15     | 3.7     | 16.9              | 5.1      | 26.8     | 100.0             | 35.0     |
| 16     | 2.3     | 16.9              | 4.6      | 15.6     | 100.0             | 25.8     |
| 17     | 0.7     | 7.3               | 1.8      | 10.5     | 83.0              | 19.5     |
| 18     | 2.4     | 13.8              | 3.2      | 25.7     | 99.3              | 28.2     |
| 19     | 3.8     | 24.9              | 6.9      | 26.1     | 100.0             | 31.6     |
| 20     | 1.0     | 12.9              | 2.9      | 7.6      | 76.9              | 14.6     |
| 21     | 1.2     | 6.0               | 1.7      | 5.9      | 76.1              | 13.2     |
| 22     | 1.9     | 18.5              | 4.8      | 7.6      | 71.8              | 15.2     |
| 23     | 7.3     | 49.4              | 12.5     | 10.1     | 66.7              | 16.9     |
| 24     | 10.5    | 50.8              | 15.0     | 14.5     | 100.0             | 20.3     |
| 25     | 1.8     | 18.3              | 4.5      | 9.8      | 82.5              | 16.7     |
| 26     | 2.7     | 21.9              | 5.4      | 32.0     | 95.9              | 31.2     |
| 27     | 0.5     | 4.5               | 1.1      | 16.5     | 100.0             | 23.6     |
| 28     | 1.1     | 10.9              | 2.7      | 7.8      | 83.7              | 15.4     |
| 29     | 0.2     | 1.2               | 0.4      | 8.8      | 44.0              | 11.5     |
| 30     | 0.5     | 5.6               | 1.4      | 8.0      | 59.6              | 14.6     |

the  $i$ th region into the grade of membership of the relative stenosis. A collection of these grades of membership will define the fuzzy set called "stenosed."

The numeric value of the percentage of perfusion defect is not directly related to stenosis in a particular artery. For example, even if we know that a patient has a 100-percent left anterior descending coronary artery obstruction, the percentage of perfusion defect in anterior view segment 10 contributes in only a "fuzzy" way to the correct diagnosis. Not only the left anterior descending artery but other arteries as well supply blood to this region. Coronary anatomy is quite variable; for example, the apical region of the left ventricle may be supplied by any or all of the three major arteries. Also, collateral blood flow can cover for the loss of perfusion from an artery that is completely or partially obstructed: Communicating channels may

develop between arteries to carry blood to the myocardial territory beyond an obstruction in the major artery.

The pattern of collateral blood flow varies greatly in patients. Moreover, the amount of flow through the collateral channels may vary at different times in the same patient, depending on myocardial stresses, metabolic and neural states, and medications. Because of these factors, perfusion defect size in a specific location will not be perfectly related to the severity and site of stenosis in a given group of patients with the same type of stenosis. Nevertheless, in a large group of patients we expect to find a detectable "fuzzy" relationship.

Assuming a statistical relationship between a percentage of perfusion defect in a region and a site of coronary artery stenosis, we evaluate probability density functions. Let the random variable  $X_i$  be the percentage of perfusion defect of the  $i$ th

region and  $Y$  be the diagnosis of a patient. Then the probability density functions are defined as

$$f_i(x) = Pr(X_i = x | Y = 0)$$

and

$$g_i(x) = Pr(X_i = x | Y = 1)$$

where  $0 \leq x \leq 100$ . Here  $Y = 0$  if the patient has "normal" coronary arteries, and  $Y = 1$  if the patient has "stenosed" coronary arteries.

We define membership function  $\mu_i(x)$ , which represents a fuzzy set called "stenosed," as follows:

$$\mu_i(x) = \frac{\int_0^x g_i(x)dx}{\int_x^{100} f_i(x)dx + \int_0^x g_i(x)dx} \quad (1)$$

The complement of the term "stenosed," which represents a fuzzy set called "normal," is

$$\mu_{i\text{comp}}(x) = 1 - \mu_i(x)$$

$$= \frac{\int_x^{100} f_i(x) dx}{\int_x^{100} f_i(x) dx + \int_0^x g_i(x) dx}$$

The above two membership functions do not represent the perfusion defect of a region but simply map the  $i$ th region of the percentage of perfusion defect into the interval  $[0,1]$ , where 0 and 1 imply that the defect represents a normal or stenosed coronary artery, respectively. Because the probability density functions are not explicitly available, we estimated them from the training data. We estimated the membership functions, in turn, through the approximate probability density functions.

To construct a fuzzy set with discrete elements, we digitize the percentage of perfusion defect. First, we find a range over which a fuzzy set is to be defined. In the simple example of the fuzzy set "tall" in the sidebar, this range was from five feet to seven feet, and the "center" element was a pair (6', 0.5). To find such a center for coronary artery disease data, we use statistics. Analysis of our training data shows that the lower values of percentage of perfusion defect are significant in discriminating between normal and stenosed arteries. For instance, the average percentage of perfusion defect for the anterior view segment 10 is 2.8 for normal patients and 32.9 for stenosed patients. Value 59.7 is the maximum percentage of perfusion defect recorded for a normal patient. Table 1 shows more statistics. According to the table, low percentages of perfusion defect might be digitized with high resolution,

**Table 2. Digitization of a percentage of perfusion defect for fuzzy set construction.**

| Range ( $L$ ) | Percent      |
|---------------|--------------|
| 1             | 0 - 1.5      |
| 2             | 1.6 - 6.2    |
| 3             | 6.3 - 13.9   |
| 4             | 14.0 - 24.9  |
| 5             | 25.0 - 38.9  |
| 6             | 39.0 - 55.9  |
| 7             | 56.0 - 76.9  |
| 8             | 77.0 - 100.0 |

and high values might be digitized with low resolution.

Using the information in Table 1, we digitize a percentage of perfusion defect,  $x$ , into eight unequally spaced ranges  $L$ :

$$L = \begin{cases} k & \text{if } 100 \left( \frac{k-1}{n} \right)^2 \\ n & \text{if } x = 100 \end{cases}$$

$$\leq x < 100 \left( \frac{k}{n} \right)^2, k = 1, 2, \dots, n$$

Table 2 shows the ranges.

The training data set consists of 64 patients: 18 with normal arteries and 46 with coronary artery stenosis. In the latter set, seven patients have stenosis in the circumflex artery, 23 in the left anterior descending artery, and 16 in the right coronary artery.

We write  $N_i(L)$  for the number of normal patients and  $M_i(L)$  for the number of stenosed patients whose percentage of perfusion defect in the  $i$ th region is  $L$ . Then, the probability density functions can be evaluated:

$$f_i(L) = \frac{N_i(L)}{\sum_{j=1}^8 N_i(j)}, g_i(L) = \frac{M_i(L)}{\sum_{j=1}^8 M_i(j)}$$

The corresponding distribution functions are

$$F_i(L) = \frac{\sum_{l=1}^L N_i(l)}{\sum_{j=1}^8 N_i(j)}, G_i(L) = \frac{\sum_{l=1}^L M_i(l)}{\sum_{j=1}^8 M_i(j)} \quad (2)$$

Table 3 shows an example function for anterior view segment 10, as derived from the training data. These functions are based on the distributions of the sample population.

Once we establish the distribution functions, we define the corresponding fuzzy sets from the discrete form of Equations 1 and 2. Then the membership functions become

$$\mu_i(L) = \frac{G_i(L)}{G_i(L) + 1 - F_i(L)}$$

$$= \frac{\sum_{j=1}^8 N_i(j) \sum_{l=1}^L M_i(l)}{\left( \sum_{j=1}^8 N_i(j) \sum_{l=1}^L M_i(l) + \sum_{j=1}^8 N_i(j) \sum_{l=1}^L M_i(l) - \sum_{l=1}^L N_i(l) \sum_{j=1}^8 M_i(j) \right)}$$

We obtained fuzzy sets for all 30 regions. As an example, Table 4 gives the fuzzy set corresponding to the example in Table 3.

**Table 3. Probability density function for anterior view segment 10.**

| Range ( $L$ ) | 1     | 2     | 3     | 4     | 5     | 6     | 7     | 8     |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------|
| $N_{10}(L)$   | 9     | 1     | 3     | 3     | 0     | 2     | 0     | 0     |
| $M_{10}(L)$   | 3     | 1     | 6     | 6     | 3     | 6     | 9     | 12    |
| $f_{10}(L)$   | 0.500 | 0.056 | 0.167 | 0.167 | 0.000 | 0.111 | 0.000 | 0.000 |
| $g_{10}(L)$   | 0.065 | 0.022 | 0.13  | 0.13  | 0.065 | 0.13  | 0.197 | 0.26  |

**Table 4. Fuzzy set for anterior view segment 10, described in terms of its membership function  $\mu(\cdot)$ .**

| Range ( $L$ ) | 1     | 2     | 3     | 4     | 5     | 6     | 7     | 8    |
|---------------|-------|-------|-------|-------|-------|-------|-------|------|
| $F_{10}(L)$   | 0.500 | 0.556 | 0.723 | 0.89  | 0.89  | 1.00  | 1.00  | 1.00 |
| $G_{10}(L)$   | 0.065 | 0.087 | 0.217 | 0.347 | 0.412 | 0.542 | 0.739 | 1.00 |
| $\mu_{10}(L)$ | 0.115 | 0.164 | 0.439 | 0.759 | 0.789 | 1.00  | 1.00  | 1.00 |

## Classification rules

1. If left lateral 5, left lateral 6, and left lateral 9 are stenosed, then the stenosis is in LAD.
2. If anterior 4, anterior 7, and left lateral 6 are stenosed, then the stenosis is in LAD.
3. If anterior 9, anterior 10, and left anterior oblique 5 are stenosed, then the stenosis is in LAD.
4. If anterior 5, anterior 6, and left lateral 8 are stenosed, then the stenosis is in RCA.
5. If anterior 9, left anterior oblique 5, and left anterior oblique 6 are stenosed, then the stenosis is in RCA.
6. If anterior 7, left lateral 4, and left anterior oblique 4 are stenosed, then the stenosis is in CCX.
7. If left lateral 2, left lateral 8, and left anterior oblique 4 are stenosed, then the stenosis is in CCX.
8. If left lateral 4, left lateral 8, and left anterior oblique 9 are stenosed, then the stenosis is in RCA.
9. If anterior 2, anterior 3, and anterior 7 are stenosed, then the stenosis is in CCX.
10. If left lateral 5, left lateral 6, and left lateral 10 are stenosed, then the stenosis is in LAD.
11. If anterior 9, left lateral 4, and left lateral 8 are stenosed, then the stenosis is in RCA.
12. If anterior 4, left lateral 1, and left lateral 5 are stenosed, then the stenosis is in CCX.
13. If anterior 7, anterior 10, and left lateral 5 are stenosed, then the stenosis is in LAD.
14. If anterior 7, left lateral 5, and left anterior oblique 6 are stenosed, then the stenosis is in RCA.
15. If anterior 9, anterior 10, and left lateral 9 are stenosed, then the stenosis is in CCX.

**Figure 2. Fifteen rules generated from the training set.**

**Table 5. Possible outcomes of tests for hypotheses.**

|                     | Test Positive   | Test Negative   |
|---------------------|-----------------|-----------------|
| Hypothesis positive | True positives  | False negatives |
| Hypothesis negative | False positives | True negatives  |

**Table 6. Performance results with data for 27 test patients (the whole numbers are percentages).**

|                          | Normal     | RCA        | CCX        | LAD         |
|--------------------------|------------|------------|------------|-------------|
| Sensitivity <sup>1</sup> | 100 (7/7)  | 71 (5/7)   | 100 (3/3)  | 70 (7/10)   |
| Specificity <sup>2</sup> | 90 (18/20) | 95 (19/20) | 92 (22/24) | 100 (17/17) |
| Accuracy <sup>3</sup>    | 93 (25/27) | 89 (24/27) | 93 (25/27) | 89 (24/27)  |

<sup>1</sup> (true positive/hypothesis positive); <sup>2</sup> (true negative/hypothesis negative);

<sup>3</sup> ((true positive + true negative)/total)

## Rule generation

We used the data on the percentage of perfusion defect, converted into fuzzy sets, to generate inductive rules to diagnose patients as having stenosis in the circumflex artery, right coronary artery, or left anterior descending artery, or as being normal.

A candidate rule for a given test set divides the sample data into two groups, positive and negative. All patients in the positive group have the same coronary artery disease; in other words, there must be no false positive in the group. The negative group may include patients with stenosis in different coronary arteries. Both true and false negative examples can reside in a negative group produced by the candidate rule. This set of negative examples is used to generate the next candidate rule. Because a candidate rule does not produce false positive examples, eventually a finite set of rules will classify training data without any mistakes.

At the beginning of the procedure, we divide the training data set (the initial target set) into four groups: normal, LAD (stenosis in the left anterior descending artery), RCA (in the right coronary artery), and CCX (in the circumflex artery). Each iteration of the procedure produces both a rule and the reduced target set for the next iteration. Each rule may contain several features as its conditions. If a rule contains too many features, it becomes too specific. If it contains too few features, it becomes too general. We tried combinations of small numbers of features — namely, two, three, and four — in rules. The best results came

from a combination of three features. In the sketch of the procedure (and the rules in Figure 2) the number following the view indicates the view segment (see Figure 1). Here is the procedure:

(1) For all combinations of three features, perform steps 2 and 3.

(2) For a choice of three features, test whether they group patients with the same kind of stenosis. For example, if an LAD group has left lateral 1, left lateral 10, and left anterior oblique 1 “stenosed” (regions 11, 20, and 21 of the whole scan) and none of the other groups (RCA, CCX, and normal) have the same features, then left lateral 1, left lateral 10, and left anterior oblique 1 form a rule for LAD.

(3) For each choice of features, count the number of patients who satisfy this rule and assign that number as an index associated with this rule.

(4) If there is more than one choice, find a rule with a corresponding maximum index. All patients' data “covered” by this rule are deleted from the target set. The reduced data set becomes the new target set for the next iteration.

This procedure generates a series of rules that classify the training data set without including false positive examples for any category. Thus, the accuracy with the training set is 100 percent. Our procedure uses a concept very similar to the AQ algorithms described by Michalski et al.,<sup>6</sup> which generate inductive decision rules from a set of examples. Using our procedure, we obtained the 15 rules listed in Figure 2.

**Table 7. Performance results for all patients using the Bayesian approach (in percent).**

|             | Normal | RCA | CCX | LAD |
|-------------|--------|-----|-----|-----|
| Sensitivity | 72     | 88  | 82  | 100 |
| Specificity | 90     | 84  | 64  | 97  |

**Table 8. Performance results for all patients using the Dempster-Shafer theory of evidence (in percent).**

|             | Normal | RCA | CCX | LAD |
|-------------|--------|-----|-----|-----|
| Sensitivity | NA     | 96  | 100 | 97  |
| Specificity | NA     | 100 | 85  | 100 |

## Results

We applied the rules to the data of 27 test patients: 10 LAD, seven RCA, three CCX, and seven normal patients. Table 5 shows the possible outcomes of tests for hypotheses. We used measures of sensitivity, specificity, and accuracy to summarize system performance. Table 6 gives the definitions of these measures and the results obtained from the test data.

For loose comparison, Tables 7 and 8 give the sensitivity and specificity results for two expert systems whose recognition rules were specified by cardiologists, not generated from data. As a consequence, the rules were applied to the whole data set of 91 patients to check the performance of the Bayesian method,<sup>1</sup> and only to the 66 patients with coronary stenosis to check the performance of the Dempster-Shafer method.<sup>2</sup> Therefore, we cannot directly compare the performance of our fuzzy set method with the performance of these two methods: The fuzzy set system was trained on 70 percent of the data, and the result is shown for the remaining 30 percent — which amounts to only 27 patients.

**O**ur method uses the concept of fuzzy sets to represent the uncertainty inherent in thallium-201 scintigrams. Cardiologists routinely analyze such scintigrams visually to diagnose which artery (if any) is obstructed. In the studies whose performance is summarized in Tables 7 and 8, cardiologists specified 68 rules for recognition of stenosed patients only. The advantage of our method is obvious. The 15 simple rules have a performance comparable with that of an experienced cardiologist.

The reliability of the rules depends on the amount of sample data from which they are generated — the larger the training data sample, the more reliable the rules. The method we presented here is a stand-alone system that could be incorporated into an expert system to generate production rules for its knowledge base. ■

## Acknowledgments

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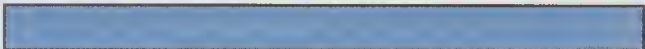
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# A Neural Network Expert System for Diagnosing and Treating Hypertension

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**C**omputer-based medical systems are playing an increasingly relevant role in assisting both diagnosis and treatment. When designing such tools, certain objectives must be considered carefully. First of all, physicians should be able to use low-cost, user-friendly instruments — for example, programs running on personal computers. Nevertheless, to satisfy physicians' requirements, processing time should be short.

Since any failure of such tools could prove harmful to patients, fault tolerance and reliability are the most crucial characteristics. At the same time, end users must be provided with as much information as possible about how the processing is carried out.

In the effort to reach these objectives, developers of computer aids for physicians face a variety of problems deriving from the complex nature of biological data. Such data is characterized by an intrinsic variability that can occur as the result of spontaneous internal mechanisms or as a



**Artificial neural networks provide effective solutions to the problems encountered in building systems that emulate a physician's expertise.**

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reaction to occasional external stimuli. Furthermore, most biological events result from the interaction of many systems and subsystems whose different effects are almost indistinguishable.

Clinicians are accustomed to such problems, but their skills cannot easily be incorporated into computer programs. Most clinical decisions are based on experience as well as on complex inferences and extensive pathophysiological knowledge. Such experience cannot be condensed into a small set of relations, and this limits the performance of algorithmic approaches to many clinical tasks. The breadth of clinical knowledge is an obstacle to the creation of symbolic knowledge bases comprehensive enough to cope with the diverse exceptions that occur in practice.

Experience-based learning, fault tolerance, graceful degradation, and signal enhancement are properties of artificial neural networks that make them effective in solving the above problems. This points to a way for implementing reliable computer-based medical systems that can closely emulate a physician's expertise.

This article describes Hypernet (Hypertension Neural Expert Therapist), a neural network expert system for diagnosing and

# Hypertension diagnosis and treatment

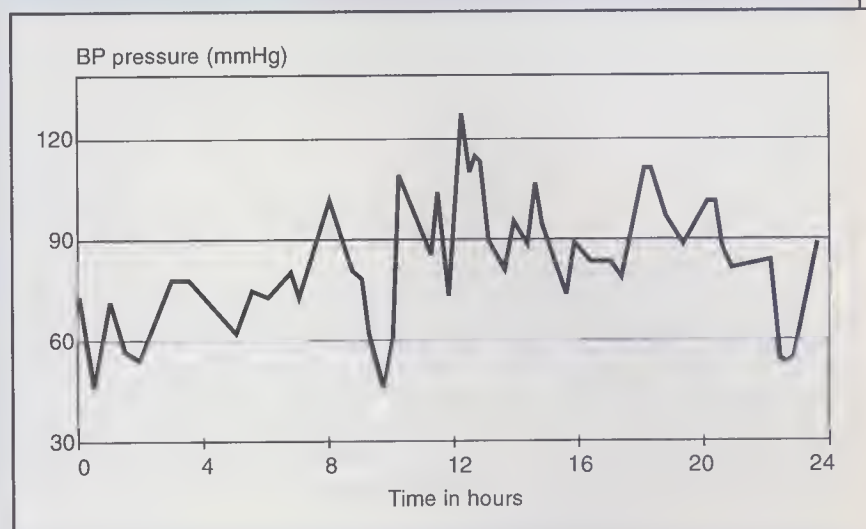
Hypertension represents a wide-spread pathological condition occurring in about 15-20 percent of the world's population. It is usually defined as the presence of a sustained elevation of the diastolic blood pressure above a 90-mmHg (millimeters of mercury) limit, at repeated, casual measurements.<sup>1</sup>

This definition leads to a diagnostic approach that can provide both false positives and false negatives. These derive mainly from disregarding the large, spontaneous, and reactive blood-pressure variations that occur during the day.<sup>2</sup>

Blood-pressure temporal dynamics are evident even on a first inspection of blood-pressure time series. The figure at right shows the plot of the diastolic blood-pressure data of a hypertensive subject, recorded with a noninvasive, automatic, ambulatory blood-pressure monitor.

These dynamics should be considered when defining blood-pressure ranges for healthy and hypertensive subjects; and time-varying reference limits, depending on the subject's sex and age, should be adopted. This would lead to a more accurate definition of the severity of hypertension.<sup>3</sup> In the absence of clear blood-pressure alterations, signs of target-organ damage or the presence of concurrent diseases should be considered.

The ideal hypotensive treatment should remove the source of hypertension. Unfortunately, for most hypertensive patients, no known cause can be found. Therefore, treatment is generally



Plot of the diastolic blood-pressure time series of a hypertensive subject.

chosen with the intent of obtaining the best control of blood-pressure values and the lowest incidence of unwanted effects.

Temporal localization and other features of blood-pressure excesses can be used as a guide for timing and dosage of antihypertensive drugs. With the proper choice of administration time, drugs can produce their maximal effect during the highest blood-pressure excesses. This optimization also leads to a reduction in the overall daily dosage of the drugs.

At present, four classes of drugs are generally accepted as first-line drugs to start hypotensive treatment: diuretics, beta-adrenoceptor-blocking drugs, angiotensin-converting-enzyme inhibitors, and calcium-channel-blocking drugs. All these drugs are effective, relatively safe, and generally well tolerated; however, some pathological conditions con-

traindicate the use of one or more.

When a pronounced hypotensive action or the reduction of specific side effects is needed, the association of different drugs can be advised.

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treating hypertension. Hypernet was developed through the cooperative efforts of the Department of Electronic Engineering of the University of Florence, the Interuniversity Center of Clinical Chronobiology, and the CNR Institute of Clinical Physiology.

After a brief look at artificial neural networks, we describe the structure of the three modules that make up Hypernet. We start with the specific problem each network is intended to solve and explain how the network is expected to operate.

The tools we have developed for implementing the system are a compiler for a simple descriptive language that enables us to define, train, and test networks; a graphic editor that translates the network drawn by the user into the proper statements; and a set of programs for interactively generating the examples.

After describing the data used as examples, the learning phase, and the results of tests for evaluating the performance of each network, we give our conclusions about overall system results.

## Artificial neural networks

Most of today's artificial neurons are based on the simple model shown in Figure 1. The model is made up of weighted connections feeding into a summation block, whose output, usually called net input, is a linear combination of the signals  $i_j$  feeding into each connection:

$$\text{net} = \sum_j w_j i_j$$

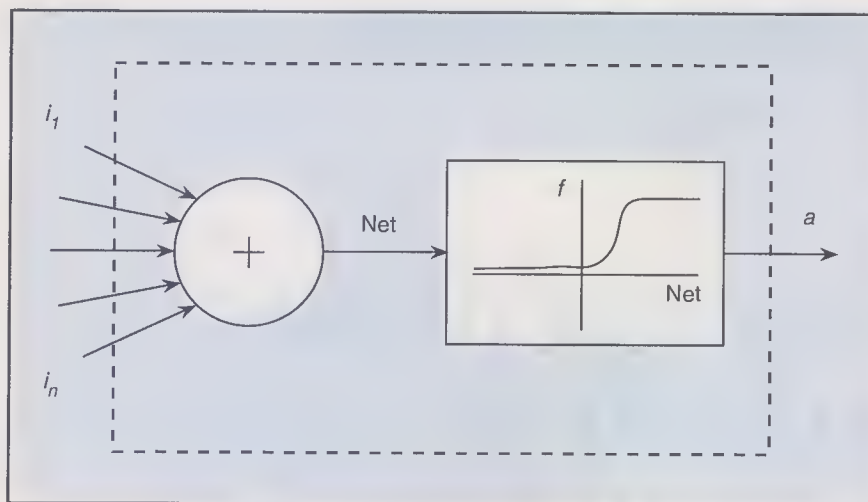


Figure 1. Functional diagram of an artificial neuron.

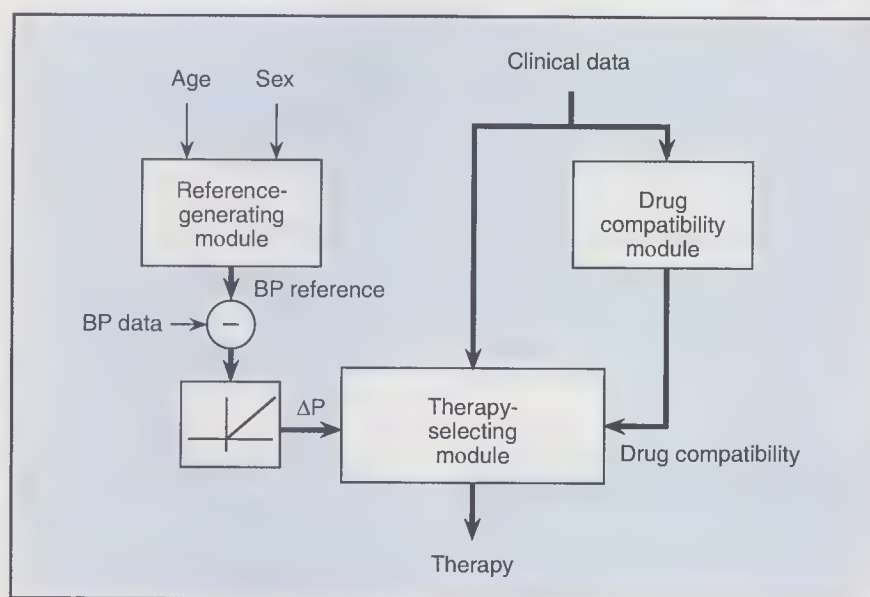


Figure 2. The logical structure of Hypernet.

where  $w_j$  is the weight associated with the  $j$ th connection.

The net input is then used as the argument for the so-called activation function whose value represents the neuron activation. This function is usually the sigmoid function

$$f(\text{net}) = \frac{1}{1 + \exp(-\text{net} - \text{bias})}$$

where bias is a term having a threshold-like effect.

A single neuron can perform simple pattern-recognition tasks, but more complex problems require connection of many processing elements to form networks.<sup>1-6</sup> Thus, PEs are usually arranged in layers and can be of three kinds: input, output, and hidden units. Input units have no processing capability; their function is to feed environmental signals to the units connected to them. Output units are neurons that emit signals toward the external world. Finally, hidden units are PEs uniquely connected to other PEs.

The networks we consider here are called feed-forward networks. This means that each unit can send its output only to units closer to the output layer.

The crucial characteristic of artificial neural systems (ANSs) is that they can learn by example to perform useful tasks. This is usually achieved by using teaching algorithms that iteratively modify the network's weights until it responds as desired to a set of input patterns (teaching inputs). This process is called supervised learning. The most widespread learning algorithm for multilayered feed-forward ANSs is the back-propagation rule, discovered by Rumelhart et al. in 1986.<sup>7</sup>

ANSs have some very useful properties. For instance, when the training set contains noisy or inconsistent examples, during the learning phase the net extracts the central tendency (or prototype) of the set. After learning, the network can generalize, giving correct responses even in the presence of patterns that are not included in the training set. In addition, thanks to the net's noise rejection capability, performance is widely insensitive to noise corrupting the input patterns. In the presence of very noisy or contradictory inputs, network performance decays gradually (graceful degradation).

Furthermore, when the input-output mapping can be obtained by applying some type of rule, the network tends to discover the rule instead of memorizing the input-output pattern pairs (though it memorizes exceptions, if any). In addition, their parallel and distributed processing characteristics (information is spread throughout the network) make ANSs widely insensitive to unit and weight deficiencies or disconnections (fault tolerance). Finally, ANSs can treat Boolean and continuous entities simultaneously.

Because of all these properties, ANSs seem highly suitable for handling the problems encountered in developing both symbolic and numerical computer tools for physicians.

## System architecture

The inputs to Hypernet are the subjects' anamnestic data and the 24-hour diastolic and systolic blood-pressure time series. System output includes four 24-item arrays, whose values specify the hourly dosage to be administered to the patient for each of the most common antihypertensive drugs. The presence and degree of hypertension (diagnosis) can be inferred from the drug

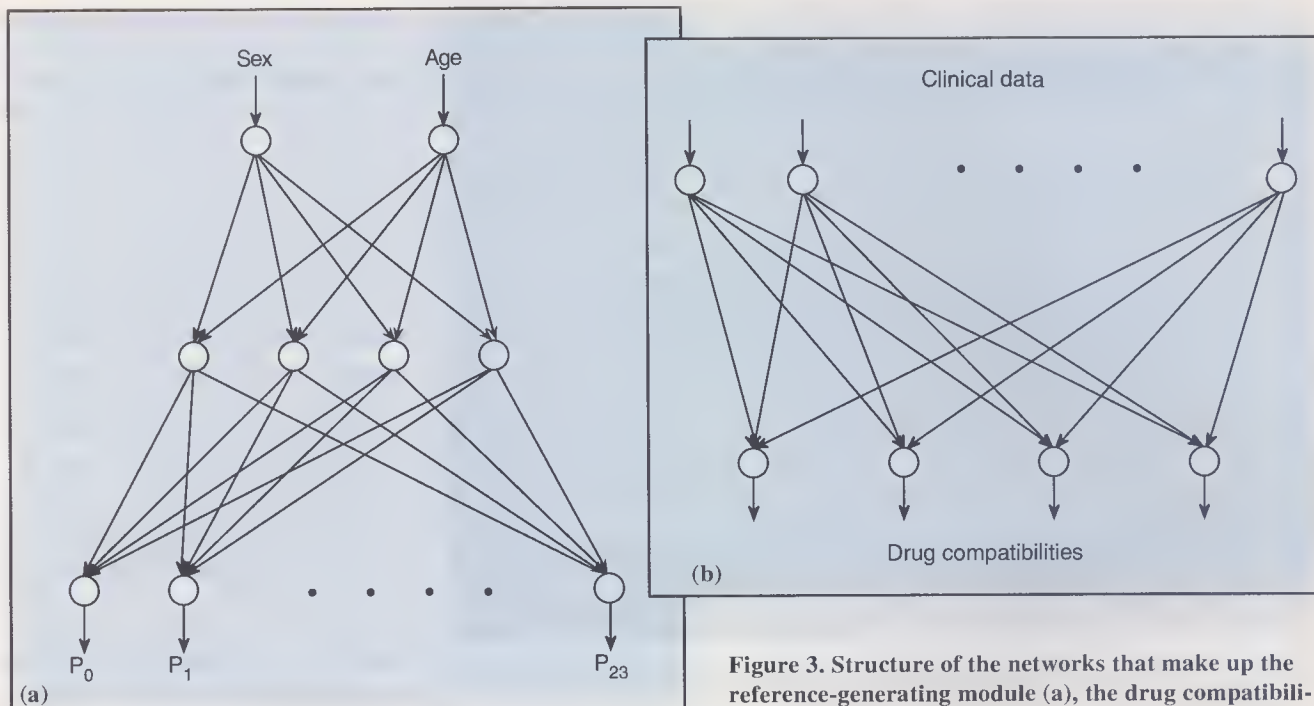


Figure 3. Structure of the networks that make up the reference-generating module (a), the drug compatibility module (b), and the therapy-selecting module (c).

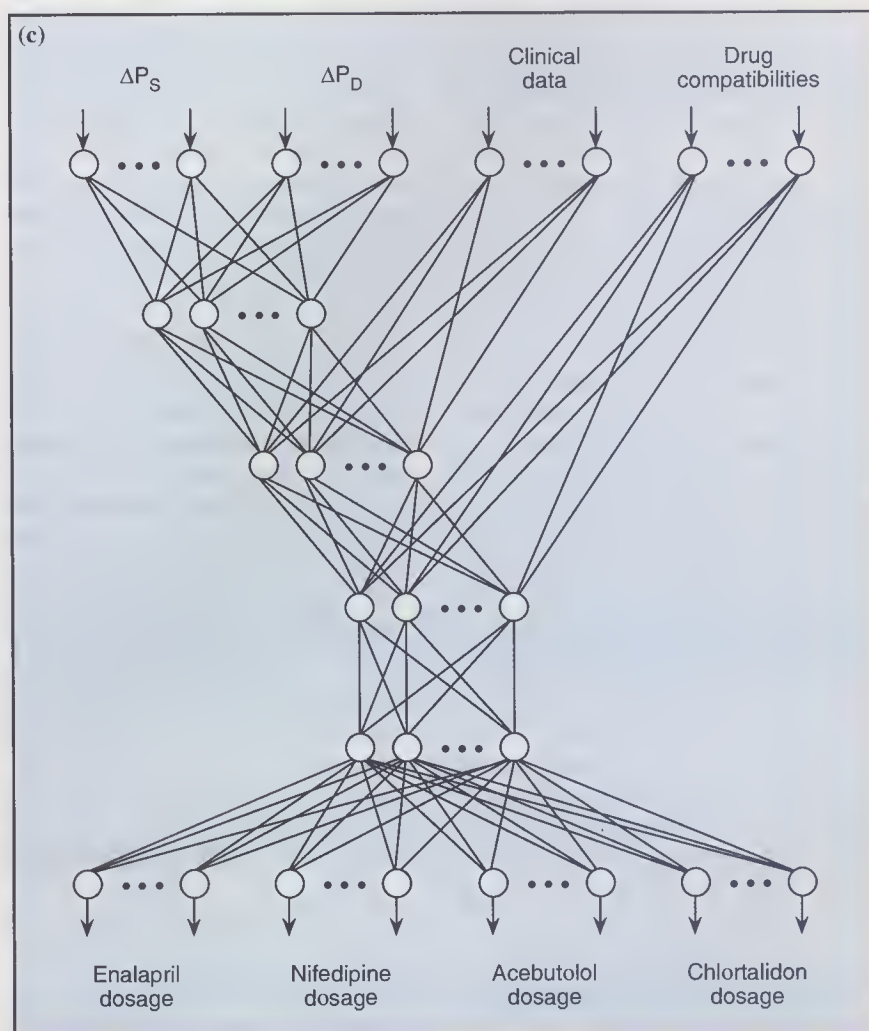
dosage: No treatment was required for normal subjects.

To simulate a physician's reasoning as closely as possible, we divided the system into three main modules (see Figure 2): the reference-generating module (RGM), the drug compatibility module (DCM), and the therapy-selecting module (TSM). Each module consists of one or two feed-forward neural networks trained by the back-propagation algorithm.

This kind of architecture increases the user's confidence in the system, providing a set of internal testing points that give explicit information about the processing. (Internal representations developed by ANNs are often too complex to be meaningful to the end user.)

The RGM comprises two identical three-layer networks, each consisting of two input, four hidden, and 24 output units (see Figure 3a). These networks compare a patient's 24-hour blood-pressure time series with the time series typical for normal subjects of the same sex and age. The purpose of this module is to call on medical knowledge regarding the concept of normality for blood-pressure recordings.

The DCM is a simple two-layer neural network having 17 input and four output units (see Figure 3b). Its function is to analyze the most important entries of the



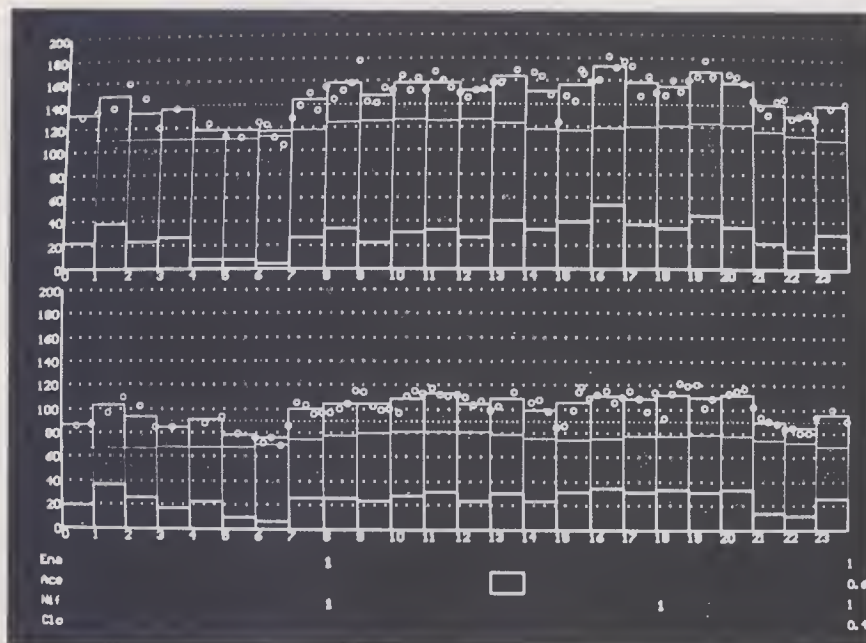


Figure 4. The display of the example-generating program for the therapy-selecting module.

patient's clinical report (inputs) and determine the patient's degree of compatibility with each considered drug (outputs). To do this, it must discover and apply the set of rules a physician usually employs for discarding unsuitable drugs.

The TSM (see Figure 3c, preceding page) is a six-layer ANS whose inputs are (1) the degrees of compatibility, (2) the differences  $\Delta P_s$  and  $\Delta P_d$  between the systolic and diastolic reference blood pressures and those derived from the patient's monitoring, and (3) five anamnestic data that can influence the diagnosis. The activations  $a_{td}$  ( $t=0, \dots, 23$  and  $d=1, \dots, 4$ ) of the 96 output units (24 values  $\times$  four drugs) of this module represent the final results of the expert-system processing:  $a_{td}$  indicates the dosage of the drug  $d$  to be prescribed at time  $t$  (all units are off if the subject is normal). The module's multilayered structure was introduced to simulate the sequence of inferences performed by the physician.

The first hidden layer comprises 12 units whose inputs are both the systolic and the diastolic  $\Delta P$ s. Its function is to integrate the pressure excesses over time and properly weight the systolic excesses with respect to the diastolic ones. Because no anamnestic data is fed into the units of this layer, the activations of such PEs form a distributed representation of the significant (sufficiently high and extended) blood-pressure excesses.

The second hidden layer includes 12 additional PEs connected both to the previous layer and to five input units representing the anamnestic data that can influence the diagnosis. This layer corrects information coming from the patient's monitoring on the basis of additional clues about hypertension.

The third hidden layer consists of 12 units whose inputs are the activations of the previous hidden layer and the four drug compatibilities estimated by the DCM. This layer, together with another 12-unit layer and the TSM's output layer, determines the patient's therapy, if needed. Three layers were used for this task because decisions about therapy require the solution of many complex problems. The network must choose the most suitable combination of drugs, considering their compatibility and the corrected pressure excesses. Furthermore, it must determine the number of administrations for each selected drug, the dosage of each administration, and the best timing.

## System implementation

To define the artificial neural networks included in Hypernet, we developed a simple symbolic descriptive language.

When the network definition file is ready, a C program we call Neural Network Com-

piler translates the language primitives into suitable data structures, and learning begins (NNC processes about 20,000 weights per second on a 20-MHz 80386 PC). After learning, NNC executes the required tests, translates the data structures into language primitives, and writes an updated network definition file on disk.

Since defining large, highly connected networks by means of such primitives may take a long time, we developed a neural network graphics editor that allows quick and user-friendly definition of very complex nets.

Even though ANS technology does not require users to be capable of programming, preparing the examples for the training set can be very complex. Therefore, we also developed some example-generating programs for converting the raw pressure data and the clinical data into language statements.

For instance, to generate the examples for the TSM, an example-generating program helps the physician integrate blood-pressure and anamnestic data with drug compatibilities for selection of the therapy. All crucial data about the patient is summarized on the graphics screen; the physician selects the timing and dosage of each drug simply by moving a cursor. As Figure 4 shows, the data includes the raw systolic and diastolic time series, their hourly averages, the reference-pressure time series, the zero-clipped differences, and the drug compatibilities.

A similar screen displays the final results of Hypernet during normal operations. The user can quickly verify the system's operation by checking the consistency of its output with the drug compatibilities, the anamnestic information, and the blood-pressure data.

## Results

The data used to train and test the networks consisted of the blood-pressure time series of about 300 clinically healthy subjects, monitored during the Italian Multicentric Study on Blood Pressure Variability, and of 85 suspect hypertensive subjects, recorded by different groups. The data for most subjects included a complete clinical report with all the information required by Hypernet.

The time series were recorded by portable automatic devices typically set to different sampling rates, depending on the time of day. To reduce the noise affecting blood-pressure measurements, and to limit the

number of inputs, we averaged blood-pressure data to obtain 24-item arrays.

Since each class of hypotensive drugs includes many medicines that are nearly equivalent, we decided to consider only the most common drug for each class so as to reduce the complexity of Hypernet. These are Enalapril, among beta-adrenoceptor-blocking drugs; Acebutolol, for angiotensin-converting-enzyme inhibitors; Nifedipine, among the calcium-channel-blocking drugs; and Chlortalidon, from the diuretics. The 17 anamnestic data influencing the choice of these drugs were used as input for the DCM; the five data affecting their dosage were used by the TSM.

The training set for the RGM included 200 examples of blood-pressure time series derived from normal males and females age 20 to 80. The number of connections in each neural network of the RGM was kept much lower than the number of data held in the training sets. Therefore, instead of simply memorizing the required mappings, the networks were obliged to discover the prototypes, of which the measured data are noisy and inconsistent instances.

During the RGM's learning phase, the networks first converged to a single prototype without regard to sex and age. The prototype was the lag-by-lag average of the 200 blood-pressure time series; every deviation from this roughly sinusoidal prototype was simply considered noise. Afterward, the networks started discovering subtler differences in the time series due to the subjects' sex and age. Figure 5 shows the after-learning output of the systolic blood-pressure net as a function of age. In addition to the known increase of the mean pressure due to aging, the net easily discovered a phase shift and an amplitude increase in the blood-pressure waveforms of older people. These are very difficult to detect with conventional statistical methods.

The DCM's training set included the anamnestic data and the drug compatibilities of 30 normal and 30 hypertensive subjects. The two-layer structure of the DCM was devised because of the simple rules physicians use to establish the compatibility of each drug. An after-learning analysis of the weights revealed that the network had actually discovered those rules.

The tests we made with a test set including 10 normal and 10 hypertensive subjects showed a correct estimation of the drug compatibilities. In particular, the network was able to grade its outputs reason-

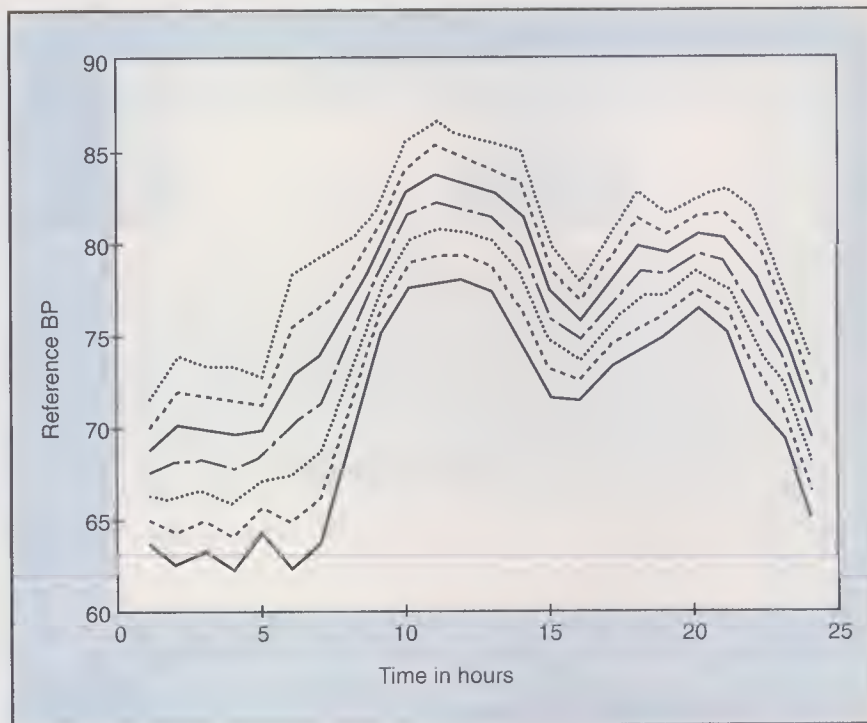


**Figure 5.** The diastolic blood-pressure-reference time series learned by the reference-generating module. Outputs are plotted for typical 20-, 30-, 40-, 50-, 60-, 70-, and 80-year-old males.

ably in the presence of anamnestic data acting on the same compatibility.

The TSM's training set included the pressure excesses, the therapy-related clinical data, and the drug compatibilities of 60 normal and 60 hypertensive subjects. Because of the dimensions (201 PEs and 2,412 weights) and the TSM's multilayered structure, the learning phase took much longer (about 50 hours of CPU time on a 20-MHz 80386 PC) than for the RGM and the DCM.

Below, to aid in understanding the learning process, are the general criteria physicians follow in treating hypertensive patients:

(1) Drugs with a 24-hour effect should be administered as single doses; drugs having a shorter effect should be administered up to three times a day. Diuretics should be limited to a single morning dose because of their action.

(2) If possible, no drug with a low compatibility should be administered.

(3) If blood-pressure excesses are spread over the entire day, a single-dose drug is preferable; otherwise, a short-effect drug is recommended. In any case, the latency

time of each drug should be considered so as to achieve the strongest effect when the maximum pressure excess is found.

(4) The time span between two administrations of the same drug should not be shorter than 6 hours.

(5) No drug should be administered during the night.

(6) When the excess is widespread during the day and is also characterized by high peaks, an association of two or more drugs should be considered.

(7) Drugs must not be administered to subjects having no significant excesses.

(8) Since the considered drugs are for oral administration (pills), quantized doses (full dose, half dose, null dose) should be prescribed.

The trained network behaves according to these rules (see Figure 6).

During training, the inhibitory effect of small blood-pressure excesses on the outputs, which leads to the implementation of rule 7, was reached in just a few iterations. Inhibitory associations were the first to be learned by the TSM. In fact, the network learned rule 2 in just a few more iterations.

The same plasticity was shown in learn-

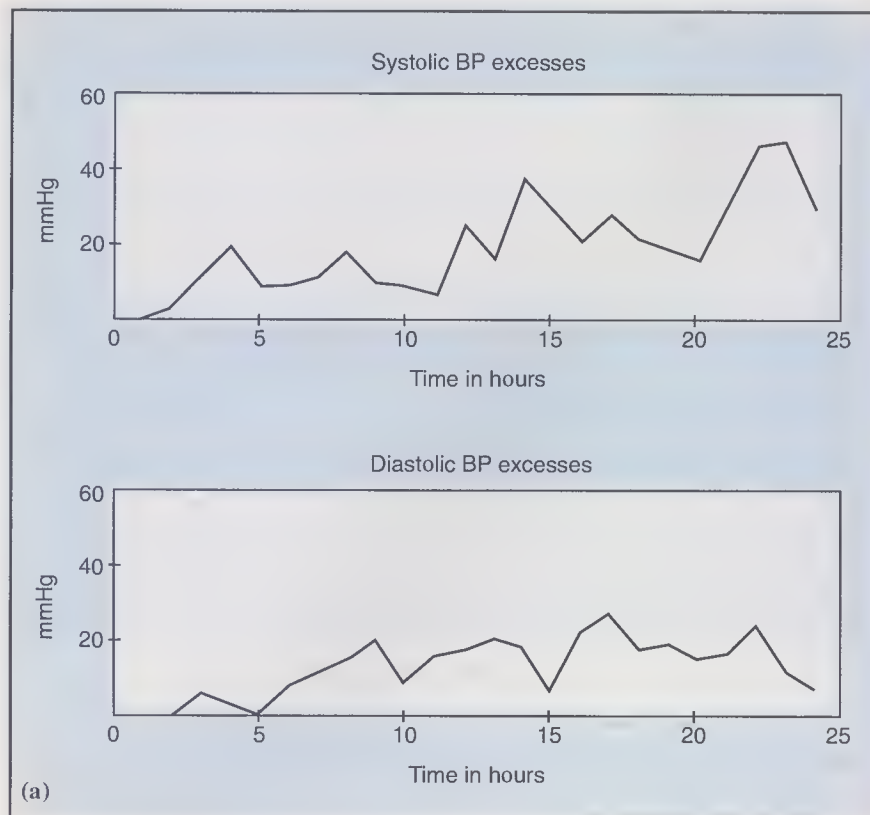
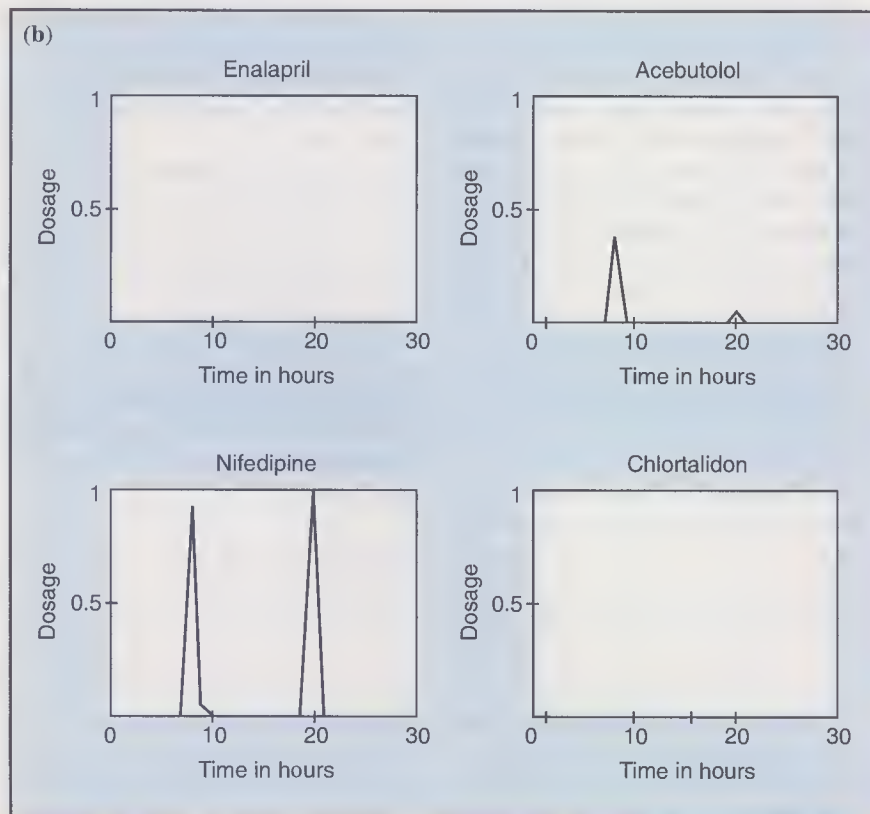


Figure 6. Plot of the blood-pressure excesses of a hypertensive patient (a) and the corresponding output of Hypernet (b).



ing rules 1, 3, 4, 5, and 8. All outputs quickly reached values close to 0, 0.5, or 1; narrowed their widespread peaks; and finally became almost impulsive, correctly located, and correctly spaced (see Figure 6b).

When two or more drug associations are equally suitable according to the patient's anamnesis, the physician's choice is characterized by high unpredictability, though it is usually biased toward a favorite solution. Therefore, discovering rule 6 required many more iterations.

Since the TSM was designed to process data derived mostly from the RGM and the DCM, we resorted to using the outputs of such modules to train and test the TSM. Therefore, the results of the tests made on the TSM can be attributed to Hypernet as a whole.

System performance was evaluated on the basis of its accuracy in both diagnoses and prescriptions. The test set included 35 subjects: 10 had neither blood-pressure excesses nor signs of target-organ damage; 25 were suspect hypertensive subjects. A diagnosis was judged correct if the system and the specialist agreed on treating or not treating. The specialist evaluated Hypernet's diagnoses as follows:

|              | Correct | Wrong |
|--------------|---------|-------|
| Treat        | 11      | 1     |
| Do not treat | 22      | 1     |
| Total        | 33      | 2     |

Hypernet correctly diagnosed 33 subjects out of 35 (94 percent), showing 92 percent sensitivity and 96 percent specificity.

For the 11 correctly diagnosed cases, the physician evaluated the treatment that the system prescribed. Treatment was judged correct in seven cases, acceptable in two, and wrong in two. (The physician found "acceptable" those treatments that could produce the needed effects, though they differed from his own advice.) So, 82 percent of the system's prescribed treatment was deemed correct or acceptable.

**C**learly, Hypernet cannot be considered a classical expert system. Knowledge is not coded in symbolic form (frames, rules, etc.) but is distributed throughout the nets. Therefore, no simple explanation module can be designed to describe how the system reaches its conclusions. Furthermore, once the networks have been trained, the knowledge embedded in the system cannot be modified without additional learning.

On the other hand, the training set itself can be considered a kind of knowledge base that can be easily consulted and modified by means of simple database programs. Furthermore, subdividing the system into modules gives users clear insights regarding the internal representations.

Judging from the results given above, the system seems highly reliable. In addition, it shows the typical speed and noise-rejection properties of ANNs. For example, its performance decays gracefully in the presence of inputs corrupted by measuring or typing errors. Furthermore, given the anamnestic data, Hypernet takes less than 1 second to reach its conclusions.

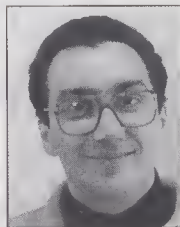
We found the results most encouraging. Nevertheless, we continue to collect new data, which will soon be available to enrich both the training and the test set. ■

## Acknowledgments

This study was supported by grants from the Regione Toscana (Ricerca Sanitaria Finalizzata 22-174/C).

## References

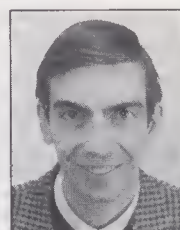
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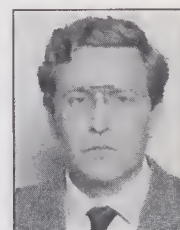
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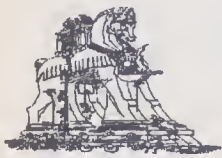
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# 1991 IEEE Symposium on Research in Security and Privacy

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## Sunday, May 19, 1991

4:00-6:30 pm **Registration Material Available, Reception**

## Monday, May 20, 1991

8:45-9:00 am **Welcome, Introduction**  
*Dan Schnackenberg, General Chair*  
*Teresa Lunt, Program Co-Chair*

9:00-10:30 am **Covert Channels I**  
*Dick Kemmerer, Chair*  
An Analysis of Covert Timing Channels,  
*John Wray*  
Reducing Timing Channels by Fuzzy Time,  
*Wei-Ming Hu*  
Toward a Mathematical Foundation for  
Information Flow Security, *James W. Gray III*

10:30-11:00 am Break

11:00-12:00 noon **Covert Channels II**  
*Steve Lipner, Chair*  
Covert Flow Trees: A Technique for Modeling  
the Direct and Inferred Recognition of Shared  
Resource Attributes Used in Covert Storage  
Channels, *Richard A. Kemmerer, Phil Porras*  
Storage Channels in Disk Arm Optimization,  
*Paul A. Karger*

12:00-1:30 pm Lunch

1:30-3:00 pm **Models**  
*Jeremy Jacob, Chair*  
Modeling Nondisclosure in Terms of the Subject-  
Instruction Stream, *James G. Williams*  
A Separation Model for Virtual Machine  
Monitors, *Nancy L. Kelem, Richard J. Feiertag*  
Safety Analysis for the Extended Schematic  
Protection Model, *Paul Ammann, Ravi Sandhu*  
A Taxonomy for Information Flow Policies and  
Models, *Simon Foley*

3:00-3:30 pm Break

3:30-5:00 pm **Distributed Systems**  
*Morrie Gasser, Chair*  
Intrusion Tolerance in Distributed Computing  
Systems, *Yves Deswarte, Laurent Blain,*  
*Jean-Charles Fabre*  
Verification of Secure Distributed Systems in  
Higher Order Logic: A Modular Approach Using  
Generic Components, *Jim Alves-Foss*  
Applying a Theory of Modules and Interfaces to  
Security Verification, *Simon S. Lam,*  
*A.U. Shankar, Thomas Woo*

5:30-7:30 pm **Reception**

8:00 pm-12:00 am **Poster Sessions, Hospitality Suite**

## Tuesday, May 21, 1991

9:00-10:30 am **Protocol Verification**  
*John McLean, Chair*  
The Use of Logic in the Analysis of Crypto-  
graphic Protocols, *Paul Syverson*  
Exploring the BAN Approach to Protocol  
Analysis, *Einar Snekkenes*

10:30-11:00 am Break

11:00-12:00 noon **Policy**  
*Earl Boebert, Chair*  
Toward an Approach to Measuring Software  
Trust, *Ed Amoroso, Thu Nguyen, Jon Weiss,*  
*John Watson, Pete Lapiska, Terry Starr*  
On the Buzzword 'Security Policy',  
*Daniel F. Sterne*

12:00-1:30 pm Lunch

1:30-3:00 pm **Authentication**  
*Cathy Meadows, Chair*  
Sphinx: Global Authentication Using Public Key  
Certificates, *Joseph J. Tardo,*  
*Kannan Alagappan*  
Protecting Security Information in Distributed  
Systems, *Asmund Skomedal, Leif Nilsen,*  
*Claus Fritzner*  
An Analysis of the Proxy Problem in Distributed  
Systems, *Vijay Varadharajan, Stewart Black,*  
*Phillipe Allen*

3:00-3:30 pm Break

3:30-5:00 pm **Information Theory**  
*Jon Millen, Chair*  
Variable Noise Effects Upon a Simple Timing  
Channel, *Ira S. Moskowitz*  
The Turing Test and Non-Information Flow,  
*Randy Brown*  
Panel: Information Theory in Computer Security,  
*Panel Chair: Gerald Eizenberg*  
*Panelists: Todd Wittbold, Tom Berson,*  
*James Gray*

5:00-6:00 pm **Technical Committee Business Meeting**

8:00 pm-12:00 am **Poster Sessions, Hospitality Suite**

## Wednesday, May 22, 1991

9:00-10:15 am **Database Security**  
*Cristi Garvey, Chair*  
Microdata Disclosure Limitation in Statistical  
Databases: Query Size and Random Sample  
Query Control, *George T. Duncan,*  
*Sumitra Mukherjee*  
Discretionary Access Controls in a High-  
Performance Object Management System,  
*Udo Kelter*  
A Novel Decomposition of Multilevel Relations  
into Single-Level Relations, *Sushil Jajodia,*  
*Ravi Sandhu*

10:15-10:30 am **Presentation of Awards**

10:30-11:00 am Break

11:00-12:00 noon **Intrusion Detection**  
*Teresa Lunt, Chair*  
The SRI IDIS Statistical Anomaly Detector,  
*Harold S. Javitz, Alfonso Valdes*  
An Information and Privilege Flow Model for  
Intrusion Detection, *Shiuhpyng Winston Shieh*  
Directed-Graph Epidemiological Models of  
Computer Viruses, *Jeffrey O. Kephart,*  
*Steve R. White*

12:00 **Symposium Adjourns**

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## Internationalizing software engineering standards

*D. Vera Edelstein, Roger Fujii, Craig Guerdat, and Pasquale Sullo\**

Demand for the products of the information processing industry — hardware, software, and services — has shown unrelenting growth on a global scale. The software industry in particular is booming.

International Data Corp. estimated 1990 worldwide sales as high as \$120 billion, with explosive growth predicted for the European market.<sup>1</sup> (Actual sales figures for 1990 were not available at press time.) But markets and technologies are not static, and competition will become global. Software producers who command significant market share will retain their predominance only if they maintain product quality and innovation, continue to lower costs, and become more customer-oriented. This will require the ability to customize applications in increasingly networked environments and to provide other individualized services.

The accelerating impetus for common international software engineering standards will undoubtedly affect the software industry. These standards may hinder the capability of individual companies to market software products and services in worldwide markets. The European Council 92 has stated its intent to adopt and enforce international standards, including a common set of software engineering standards, for all 12 member nations of the European Economic Community. Given the immensity of this market — larger than that of the US — vendors outside Western Europe will have little choice but to conform to EEC-sanctioned standards. Enforcement will include requirements for product certification and warranty, and purchasers may require certified compliance as a contractual element.

**Generic models.** Standards develop at multiple levels, addressing varying con-

cerns ranging from the very abstract to the final technical details. Generic (abstract) models establish conceptual frameworks and basic terminology. Technical standards typically evolve in more and more finite detail, describing specific implementations of the generic model.

Two significant examples of these generic standards efforts are illustrated by the Open Systems Interconnection (OSI) standard, and the 9000 Series standards adopted by the International Organization for Standardization (ISO).

**Open systems.** Internationally, a strong and growing emphasis on the open systems approach tends to avoid reliance on the proprietary systems of vendors.<sup>2</sup> The Open Systems Interconnect model, by establishing and defining a set of distinct layers involved in information transaction processing, has provided a basis for organizing and standardizing process interactions.

Many countries and major computer vendors have adopted — or intend to adopt — some form of the OSI model, and more detailed technical standards are being formulated by international consensus for interfaces between layers of this model.

In the US, the Government OSI Profile (GOSIP) initiative mandates that, as of August 1990, procurements must conform to OSI conventions. Such companies as IBM and DEC have announced their intentions to support OSI standards. Yet, a great many de facto standards based on existing technologies remain despite rapidly growing interest in OSI among consumers who have been captive to vendor-proprietary architectures and standards.

Software producers who fail to respond to these shifting market dynamics may find themselves bested by emergent competitors ready and willing to adapt and develop products that meet the new requirements. Proprietary systems are not likely to disappear, but the open systems concept is the wave of the future, bring-

ing with it vastly broader opportunities for competition in the development of software-based systems.<sup>3</sup>

**The ISO 9000 Series.** Another international imperative that will affect software development is the standardization of quality management systems. Customers have increasingly stringent expectations for quality in products and services of all kinds.

There has been a growing realization among the world's producers, service providers, and consumers that product quality derives mostly from process quality. Producers who are seriously trying to achieve quality improvements often find their efforts negated by unreliable suppliers. They, as customers, are demanding assurance that their suppliers can effectively control, maintain, and continually improve the quality of the products and services upon which they depend.

Software suppliers, providing what has become a crucial, integral element of most modern products, may soon find themselves having to demonstrate the capability of their development processes and methods.

The ISO has introduced its ISO 9000-9004 Series of Quality Management and Quality Assurance Standards.<sup>4</sup> This series, which has been adopted by the European Council and many other countries, represents a concise, generic description of the essential elements of management systems for assuring quality in development, production, and qualification with emphasis on the "what" over the "how." Specific methodologies are left to the user, but the standards require documentation and demonstrable efficacy.

Applicability of the ISO 9000 Series is not limited to manufactured products. A software version of ISO 9001, "Part 3: Guidelines for the Application of ISO 9001 to the Development, Supply, and Maintenance of Software," was approved by international ballot and adopted by Technical Committee 176 at its annual plenary session last November.

\* Edelstein and Guerdat are with Nynex; Fujii, with Logicon Inc.; and Sullo, with Nynex and Rensselaer Polytechnic Institute.

Purchasers can require compliance (including delivery, installation, and service) with the ISO 9000 Series throughout the term of a contract. Enforced compliance could become a significant barrier to software vendors who will not or cannot document their quality management systems and demonstrate their effectiveness. Such compliance could become a marketing advantage to those who can pass the stringent audits and maintain certification.

Starting in 1992, companies in the EEC will require their suppliers to be registered under the Euro Norm 29000 Series of Standards, an ISO 9000 Series equivalent. Compliance will remain voluntary in the US and most countries outside the EEC, but voluntarism will have little practical significance if purchasers require not only compliance, but registered certification. Software developers and service providers will be greatly mistaken to assume that they will be excluded from this movement.

**Emerging technical standards.** Such imperatives as open systems and the reality of ISO 9000 are in decided contrast to the way standards were established in the past.<sup>5</sup> Previously, standards development was an evolutionary, bottom-up process, driven primarily by market dominance. Established practices of one or a few market-dominant companies became industry standards that became national standards that became international standards.

International software standardization is becoming technology driven, although it would be naive to suppose that market dominance or nationalistic/regional protectionism will not play a role in future software standardization. Globally dispersed, multinational enterprises depend on a consistent, vendor-independent codification of engineering practices for software-driven systems.

In this new environment, the technological demands for compatible media, software, consumables, and services will shape the standards, which will then guide the development of new products and processes. In this nontraditional, top-down process, participation in international standards development from the outset is a necessity.

The ISO 9000 Series and the OSI model, along with other standards efforts, establish a broad, generic framework for directing subsequent, more specific technical software standards. In addition to carrying out the activities of ISO Technical Committee 176, which is responsible for the ISO 9000 Series, and its software subcommittee SC2, the ISO and the International Electrotechnical Committee established the Joint Techni-

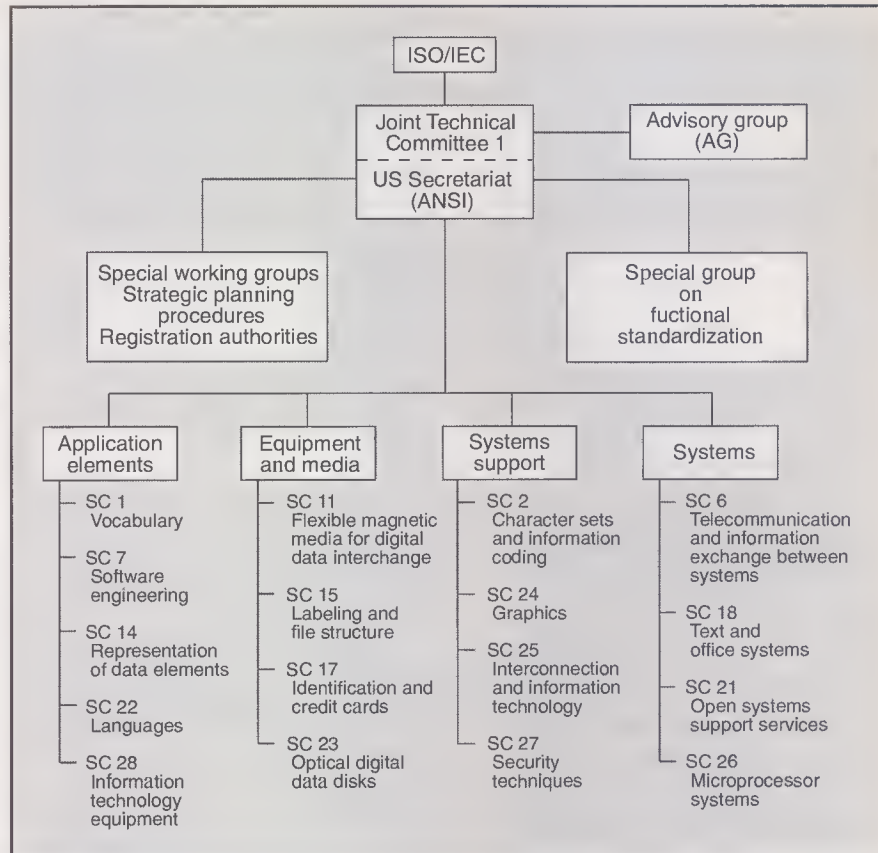


Figure 1. Organizational structure of ISO/IEC JTC1.

## Glossary

|       |                                                                              |
|-------|------------------------------------------------------------------------------|
| ANSI  | American National Standards Institute                                        |
| BSI   | British Standards Institute                                                  |
| EEC   | European Economic Community                                                  |
| EN    | Euro Norm 29000 Series of Standards                                          |
| GOSIP | US Government Open Systems Interconnect Profile                              |
| IEC   | International Electrotechnical Committee                                     |
| ISO   | International Organization for Standardization                               |
| JTC1  | Joint Technical Committee 1 on Information Technology                        |
| NIST  | US National Institute of Standards and Technology, US Department of Commerce |
| OSI   | Open Systems Interconnection                                                 |
| SC    | Subcommittee                                                                 |
| SCUSA | Standards Council of the United States of America (proposed)                 |
| SIGMA | Software Industrialized Generator and Maintenance Aids                       |
| TAG   | Technical advisory group                                                     |
| WG    | Working group                                                                |

cal Committee 1 on Information Technology in 1987 from previously existing committees.<sup>6</sup>

The more specific technical concerns of JTC1 will crucially affect the way the ISO 9000 Series will be applied to information technology. Put another way,

compliance to standards emerging from JTC1 will most likely provide direct support for compliance to ISO 9000.

*Joint Technical Committee 1.* Figure 1 illustrates the organization of JTC1 and its subcommittees. Of primary impor-

tance to software interests is Subcommittee 7, Software Engineering, whose mission is to develop, from position papers supplied by member nations, a set of standards pertaining to information systems engineering. Four working groups, each with responsibility for a particular area of software engineering, have been formed under SC7. They are

- WG1 — Symbols, charts, and diagrams
- WG2 — Software system documentation
- WG3 — Software engineering and quality management
- WG5 — Reference model for software development

WG members represent their respective member nations. However, member nations present their positions at the JTC1 level. SC7 holds an annual plenary meeting in the early part of the summer. WG meetings are usually held a few days before or after plenary sessions.

Each participating country has a single vote, typically cast by a national standards organization acting as the official representative. For example, the American National Standards Institute represents the US on JTC1 (and also serves as its administrative secretariat),

and the British Standards Institute represents Great Britain.

Since each participating member nation has only one vote, each national delegation must develop a unified position on all proposals through its home national standards organization, whatever its structure. Most member nations have domestic technical advisory groups that coordinate their participation in SC7.

Usually, these TAGs closely mirror the international model. Figure 2, for example, illustrates the US organizational structure. Note that the TAG has the same WGs as SC7.

Typical responsibilities of the domestic SC7 TAGs include

- initiating and approving positions for new standards;
- coordinating positions on drafts being circulated for approval, ISO/IEC questionnaires, plenary agenda items, reports of meetings, etc.;
- recruiting technical experts to serve on WGs;
- appointing delegation heads and nominate representatives to international meetings; and
- establishing liaisons with TAGs in related fields.

In the US, membership in the SC7 TAG is open to "any national person (or-

ganizations, companies, government agencies, individuals) who might reasonably be expected to be, or who indicate that they are, directly or materially affected by the committee's work."

The TAG meets quarterly in locations throughout the US. Delegates to the SC7 international plenaries are selected from TAG members. The US SC7 TAG sends technical experts to the international working group meetings. Those who cannot attend meetings can become "correspondent" members; such members receive all materials provided to regular participants for review and comment and, additionally, may submit items for consideration.

Adoption of an international standard takes three to five years. New proposals pass through various drafts with increasingly larger review audiences. Ultimately, a consensus draft standard is voted on by all SC7 members and then by JTC1 members. If approved, the new international standard becomes enforceable. An alternative, shorter method is to adopt a national standard, but this will occur only if participation and review by international members is sufficient during the national development process.

*Current and proposed JTC1/SC7 work items.* Development of international software engineering standards is still in its early stages. The emphasis for the next three years will be on establishing a robust and flexible foundation on which to build future standards. This initial work focuses on the definition of a common development framework with a set terminology and symbology, which entails specific compliance and certification procedures and conditions for warranty. An emphasis on process and process assessment, including metrics, is likely to affect software producers much like Department of Defense specifications affected software development in the US.

Standards projects are under way in each of the four working groups. They concern the fundamental definitions that affect software engineering and include efforts to specify

- a generalizable model of the software engineering process;
- minimal documentation expectations for computerized systems;
- development diagramming symbols and techniques;
- software life cycle processes;
- software quality characteristics and metrics; and
- technical specifications, such as requirements, designs, and tests.

Table 1 identifies projects assigned to each group and the nationality of its

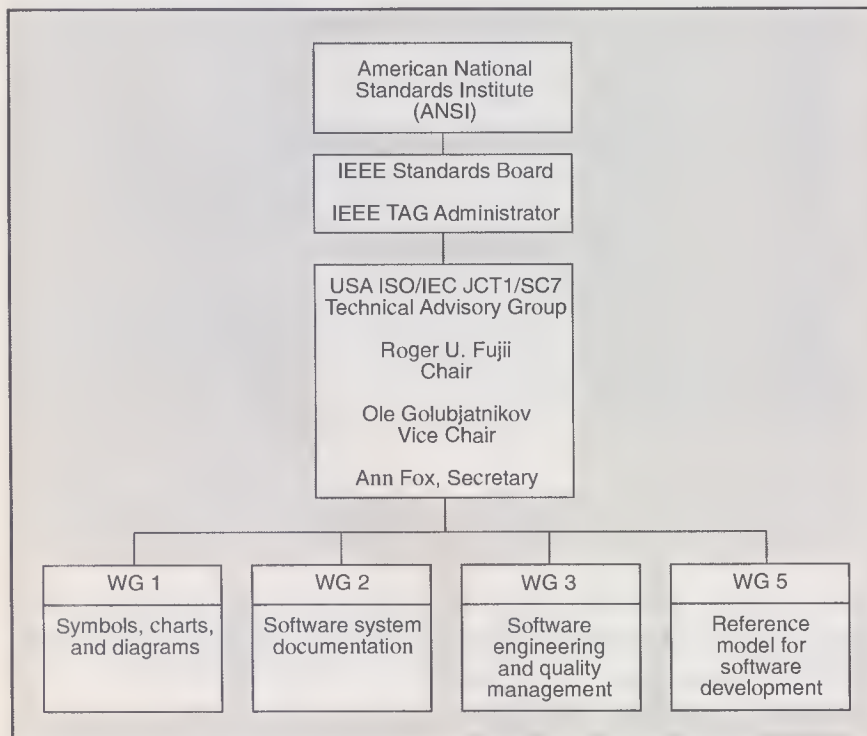


Figure 2. SC7 US TAG organization.

project editor, whose primary responsibilities are to coordinate technical content and achieve consensus.

*Anticipated impacts.* Current standards work items, if incorporated into future ISO standards, will affect software markets. Besides supporting open architectures, new standards are likely to establish procedural requirements and further specify certification criteria that will be used worldwide. Listed below, by working group, are some of the anticipated impacts of projects:

**WG1 — Symbols, charts, and diagrams**

- Specification of techniques for charting, diagramming, and using icons will affect internationally accepted CASE tools.

**WG2 — Software system documentation**

- These proposals have dealt with issues regarding acceptable standards on packaging formats for consumer software.
- New standards are being developed to describe the format of interim products of the software development process (for example, requirements specification, design description, testing documents, and user manuals).

**WG3 — Software engineering and quality management**

- These proposals form the foundation that will define the software development process and its management and control. After these proposals have been adopted (a selection will be made by the European Council for 1992), software products not developed in accordance with these standards cannot be sold to EEC countries, NATO, or others who subscribe to them.
- Many member countries want certification or warranty in conjunction with software development standards. Inability to meet certification requirements or to provide satisfactory warranties may exclude products from international, or even domestic, markets.
- Japan is the chief proponent of software quality metrics. Such metrics, if incorporated into standards, may become a basis for warranty and contractual conditions. Software developers who cannot achieve acceptable levels of measured quality will be at a competitive disadvantage.

**WG5 — Reference model for software development**

- Adopting a reference model will establish a framework for how soft-

**Table 1. Active and proposed work items.**

| Working group                                                                    | Work items                                                                                                                                                                          | Editor    |
|----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| WG1 — Symbols, charts, and diagrams<br>(Convenor: US)                            | Conceptual framework for software development diagrams                                                                                                                              | US        |
|                                                                                  | Charting techniques for software development and maintenance (process flow diagrams, state transition diagrams, data modeling diagrams, dataflow diagrams, data structure diagrams) | Japan     |
|                                                                                  | Conventions for use of symbols and icons in software systems (including software engineering tools)                                                                                 | US        |
| WG2 — Software system documentation<br>(Convenor: UK)                            | Transfer of information between life cycle phases                                                                                                                                   | Open      |
|                                                                                  | Guidelines for documentation of computer-based systems                                                                                                                              | Open      |
|                                                                                  |                                                                                                                                                                                     |           |
| WG3 — Software engineering and software quality management<br>(Convenor: Canada) | Software quality characteristics                                                                                                                                                    | Japan     |
|                                                                                  | Software life cycle management                                                                                                                                                      | US        |
|                                                                                  | Software quality management                                                                                                                                                         | US        |
|                                                                                  | Software configuration management                                                                                                                                                   | US        |
|                                                                                  | Requirements/design/testing, etc.                                                                                                                                                   | US        |
| WG5 — Reference model for software development<br>(Acting Convenor: UK)          | Evaluation and selection of CASE tools                                                                                                                                              | Open      |
|                                                                                  | Reference model                                                                                                                                                                     | UK/Canada |
|                                                                                  | Reference model overview                                                                                                                                                            | US        |
|                                                                                  | Reference model — Mapping of relevant information systems engineering standards                                                                                                     | Japan     |

ware is to be developed. Pressure is increasing among member nations to include procurement requirements and consumer usage/packaging requirements in the overall development model. This could affect software development contracts and other third-party considerations.

**The need for broad international participation.** Software development is becoming a global activity, and it will become more competitive. Players in the global market will include not only the US, Japan, and Western Europe, but also countries and regions not now highly industrialized or technology-oriented.

Eastern Europe has thousands of talented and creative software engineers and programmers, and the number of sophisticated, entrepreneurial software companies in India has been growing exponentially.

To ensure proper representation and fair treatment for all concerned parties at the international level, universal participation is mandatory.

Ideally, all segments of the computer and software establishment in the various countries should be represented. This includes industries, professional societies, government agencies, academe — even individual software professionals.

Participants will have the opportunity to present their experiences in project development and the application of state-of-the-art technologies. They will gain firsthand knowledge of pending proposals and be able to influence their development and gauge their potential impact.

Participation provides leadership, information, and feedback. Failure to participate threatens isolation from the international software community. Technological leadership and expertise will become more defined within the context of a coordinated international effort. In the long run, all nations will benefit.

In the US, the American National Standards Institute and the IEEE Computer Society provide the channel for international participation through the organizational structure described above. Participation is entirely voluntary.

The system of voluntary standards, administered by the private sector, received overwhelming reinforcement and support at a Washington, DC, hearing held last April and conducted by the US National Institute of Standards and Technology.<sup>7</sup>

The publicized aim of the hearing was to elicit comments from a broad representation of interested parties regarding a US Department of Commerce proposal to establish a "standards council of the United States of America" under the NIST. The council would create "an infrastructure to sustain a cohesive national standards system" and generally initiate various actions to improve US participation in international standards-related activities. The SCUSA model is based on Canada's national structure for international participation.

Many of those commenting on the hearing interpreted the SCUSA model as an attempt to impose governmental control over the accreditation of national standards developers and compliance certifiers and the establishment of US policies regarding international standards.

For the near future, US participation in

the international standards arena will apparently continue to be private-sector administered. Some countries have more governmental involvement.

Japan's SIGMA project, a consortium of more than 180 firms involved in establishing an integrated and standardized system for building software products, backed by the Ministry of International Trade and Industry (MITI), will undoubtedly influence Japan's position on international software engineering standards. Europe has the EEC.

Whatever the infrastructure for national participation in international software standards activities, standards emerging from JTC1 and other groups in the next three to five years will shape the direction of software technology far into the future.

## To go further

To obtain copies of ISO Standards 9000-9004, contact International Sales Dept, ANSI, 1430 Broadway, New York, NY 10018, phone (212) 354-3000.

For further information about the US ISO/IEC JTC1 SC7 TAG, contact Roger Fujii, Chairperson, US SC7 TAG, c/o Logicon Inc., 222 W. Sixth St., San Pedro, CA 90731, phone (213) 831-0611, ext. 2420, fax (213) 548-5984.

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## IEEE elects 50 Computer

The IEEE Board of Directors has completed its annual election for 1990 and conferred the title of IEEE fellow on 50 Computer Society members. A total of 403 nominations were made, from which 237 were elected. The IEEE fellow designation was effective as of January 1, 1991.

The title of fellow recognizes outstanding contributions of senior members in one or more areas. The alphabetical list below identifies the new IEEE fellows who are Computer Society members and the citation each new fellow received. The IEEE society, group, or council that evaluated the respective candidate appears in parentheses.

**Ashok K. Agrawala**, College Park, Maryland, for contributions to distributed algorithms and policies for computer systems (Computer).

**Frances E. Allen**, Yorktown Heights, New York, for contributions to the science of compiler optimization and leadership in its applications (Computer).

**Kitsutaro Amano**, Tokyo, Japan, for contributions to optical-fiber submarine cable systems and digital transmission equipment (Communications).

**Panayotis J. Antsaklis**, Notre Dame, Indiana, for contributions to the theory of feedback stabilization and control of linear multivariable systems (Control Systems).

**Mario R. Barbacci**, Pittsburgh, Pennsylvania, for contributions to computer-aided design of digital systems (Computer).

**Carleton A. Bayless**, Foresthill, California, for leadership in the planning and management of large communications networks and for leadership and contributions to professional societies (Engineering Management).

**Richard P. Brent**, Canberra, Australia, for contributions to the development and analysis of parallel algorithms (Computer).

**Joseph D. Bronzino**, Hartford, Connecticut, for contributions to biomedical and clinical engineering education, to medical ethics, and to the application of signal processing for the study of brain function (Engineering in Medicine and Biology).

**Chin-Long Chen**, Wappingers Falls, New York, for contributions to error-correcting codes for computer applications (Information Theory).

## Society members to fellow grade

**John A. Darringer**, Somers, New York, for contributions to the development of practical techniques and algorithms for automated logic synthesis of high-performance computers (Computer).

**W. Kenneth Dawson**, Vancouver, Canada, for technical leadership and contributions to the development of instrumentation bus standards and nuclear data acquisition and control systems (Nuclear and Plasma Sciences).

**Narsingh Deo**, Orlando, Florida, for contributions to graph theory, algorithms, and applications (Circuits and Systems).

**Larry E. Druffel**, Pittsburgh, Pennsylvania, for

leadership in defining and managing national software technology programs (Computer).

**Stuart I. Feldman**, Morristown, New Jersey, for contributions to software engineering and software configuration management (Computer).

**Inder S. Gopal**, Yorktown Heights, New York, for theoretical and experimental contributions to integrated networks, especially to high-speed packet switching and distributed protocols for network control (Communications).

**Bhaskarpillai Gopinath**, Watchung, New Jersey, for contributions to the modeling and analysis of communication systems (Communications).

**Jean-Paul Haton**, Vandoeuvre-Les-Nancy, France, for leadership in and contributions to automatic speech recognition (Signal Processing).

**John L. Hennessy III**, Stanford, California, for contributions to computer architecture, VLSI, and programming language design — including implementations in these fields — and for developments in reduced instruction-set computing architectures (Computer).

**Gabor T. Herman**, Philadelphia, Pennsylvania, for contributions to medical imaging, particularly in the theory and development of techniques for the reconstruction and display of computed tomographic images (Engineering in

## CS Fellows Committee chair encourages nominations for IEEE fellowship

Election to fellowship in the IEEE is a significant and rewarding experience for members of our profession. Many of our colleagues are deserving, and I encourage you to help them achieve this recognition.

The Computer Society Fellows Committee, which must endorse each nominee, is prepared to offer advice regarding the best ways to promote a candidate. Please note the eligibility requirements below. Key to a candidate's success is a crisp statement of accomplishments, the evaluation of the appropriate society or council, and the selection of references who will provide strong endorsements. A candidate must have been an IEEE member of any grade, including student member, for at least five years, and must be a senior member at the time of nomination. (Senior membership applications received by April 1, 1991, have a good chance for approval prior to the fellows nomination process.)

An optional provision allows for endorsements from IEEE entities such as sections, chapters, and committees, and from non-IEEE entities and non-IEEE individuals. Such endorsements may be useful when these entities or individuals are in the best position to provide a credible statement. Nominators need not be IEEE members, and the IEEE Guide for Fellow Grade Nominations, included in the nomination form package, states that nominations carry no more weight if the nominator is a senior member or a fellow. (Members of the IEEE Board of Directors, the IEEE Fellow Committee, or the Society Evaluation Committee cannot act as nominators or endorsers, however.)

The original typewritten 1991 nomination form must be received at IEEE headquarters by April 30, 1991, at which time a copy must also be received by the evaluating society (send to Merlin G. Smith at the address shown below). In addition, IEEE must receive at least five fellow grade

references by April 30. The evaluating society should be the one best able to evaluate the candidate's work. If a candidate's work falls under the auspices of two societies, a nominator may choose the one expected to give the best evaluation. Evaluation by the Education Society may be a beneficial option for educators.

A nomination package, complete with a nominations guide, is available from Dolores Wright, IEEE Headquarters, 345 East 47th St., New York, NY 10017, phone (212) 705-7750.

In evaluating the nominations, the IEEE Fellow Committee considers the following criteria:

- individual contribution(s) as an engineer or scientist, technical leader, or educator;
- technical evaluation by one IEEE society/council;
- tangible and verifiable evidence of technical accomplishments, such as technical publications, patents, reports, published descriptions of products, and/or services;
- confidential opinions of references who can attest to the candidate's work (in the US and Canada these references should be from IEEE fellows; outside the US and Canada, senior members may be used as references, if needed);
- service to IEEE (or AIEE or IRE); and
- total years in the profession.

If more information is needed, please contact me at the IBM T.J. Watson Research Center, PO Box 218, Yorktown Heights, NY 10598, phone (914) 945-1240, fax (914) 945-3780, Compmail m.smith, Internet merlin@ibm.com.

Your efforts will be appreciated.

*Merlin G. Smith  
Chair, Computer Society Fellows Committee*

Medicine and Biology).

**Ronald G. Hoelzeman**, Pittsburgh, Pennsylvania, for leadership and contributions to electrical and computer engineering education (Computer).

**Hirokazu Ihara**, Yokohama, Japan, for leadership in and the development of decentralized control systems and fault-tolerant computers (Computer).

**Ravishankar K. Iyer**, Urbana, Illinois, for contributions to reliable computing (Computer).

**Anil K. Jain**, East Lansing, Michigan, for contributions to statistical pattern recognition and image processing (Computer).

**Mark G. Karpovsky**, Boston, Massachusetts, for contributions to techniques and theory for designing and testing circuits and systems (Computer).

**Israel Koren**, Amherst, Massachusetts, for contributions to the field of fault-tolerant VLSI systems (Computer).

**Tosiyasu Laurence Kunii**, Tokyo, Japan, for contributions to *The Visual Computer* and visual computation (Computer).

**John C. Lindenlaub**, West Lafayette, Indiana, for contributions to instructional technology in electrical engineering (Education).

**Chao-Ning Liu**, Yorktown Heights, New York, for contributions to pattern recognition methodology and pattern-recognition-based systems (Computer).

**Jack Minker**, Bethesda, Maryland, for contributions to deductive databases, disjunctive logic programming, and artificial intelligence (Computer).

**John B. Munson**, Nassau Bay, Texas, for contributions to the software factory concept of software development (Computer).

**Arthur T. Murphy**, Wilmington, Delaware, for contributions to the analysis of electromagnetic effects in the design of high-speed electronic interconnections (Components, Hybrids, and Manufacturing Technology).

**Ramakant Nevatia**, Los Angeles, California, for contributions to the field of computer vision (Computer).

**William H. Ninke**, Holmdel, New Jersey, for contributions to image manipulation, communication, and display systems (Communications).

**Alice C. Parker**, Los Angeles, California, for contributions to design automation in the areas of high-level synthesis, hardware descriptive languages, and design representation (Circuits and Systems).

**J. Mark Pullen**, Woodbridge, Virginia, for technical leadership in computing systems and networking (Computer).

**William E. Riddle**, Boulder, Colorado, for contributions to the software design of concurrent systems and the development of supporting software tools and environments (Computer).

**Krishan K. Sabnani**, Murray Hill, New Jersey, for contributions to research and development in communication protocols (Communications).

**Hanan Samet**, College Park, Maryland, for contributions in the area of hierarchical data applications in spatial databases for computer graphics and image processing (Computer).

**Arthur C. Sanderson**, Troy, New York, for contributions to the theory of sensor-based robotic systems and its application to flexible manufacturing automation (Robotics and Automation).

**Jorge L.C. Sanz**, San Jose, California, for contributions to the theory, algorithms, and architectures of multidimensional signal processing (Signal Processing).

**Philip E. Sarachik**, Brooklyn, New York, for contributions to modern control theory (Control Systems).

**Martha Sloan**, Houghton, Michigan, for contributions to engineering education, leadership in the development of computer engineering education as a discipline, and leadership in extending engineering education to women (Education).

**W. Ross Stone**, La Jolla, California, for contributions to the fields of inverse problems and computational electromagnetics (Antennas and Propagation).

**James M. Tien**, Troy, New York, for contributions to systems engineering as applied to public systems (Systems, Man, and Cybernetics).

**Hwa-Chung Torng**, Ithaca, New York, for contributions to the architecture and design of digital systems, and engineering education (Computer).

**James H. Tracey**, San Antonio, Texas, for contributions to switching theory and computer design, and leadership in program development at universities (Computer).

**Saburo Tsuji**, Osaka, Japan, for contributions to research in computer vision and robotics (Computer).

**Benjamin Wan-Sang Wah**, Urbana, Illinois, for contributions to the field of parallel processing (Computer).

**Colin H. West**, Ruschlikon, Switzerland, for contributions to the automated validation of communication protocols (Communications).

**Masao Yano**, Hyogo-ken, Japan, for contributions to the development of static VAR compensators and static converters for industrial systems (Industrial Electronics).

## Cain elected 1991 IEEE vice president; Nagle, Read to run for 1992 president-elect

J. Thomas Cain, an associate professor of electrical engineering at the University of Pittsburgh, has been elected 1991 vice president of publication activities by the Assembly of the IEEE. Currently on the IEEE Computer Society's Publications Board, Cain also served as the society's vice president for publications in 1986 and 1987. He was the first recipient of the society's Taylor Booth Award for achievement in education in 1989.

In addition to chairing the IEEE Publication Activities Board, Cain will serve as a member of the IEEE Board of Directors and the Executive Committee.

In the IEEE's 1991 election, Computer Society members H. Troy Nagle and Wallace S. Read will run for 1992 president-elect. Nagle is a professor of electrical and computer engineering at North Carolina State University, Raleigh, North Carolina, and Read is president of the Canadian Electrical Association, Montreal, Quebec. Also set to run for

president-elect is Robert T.H. Alden, professor of electrical and computer engineering, Power Research Laboratory of McMaster University, Hamilton, Ontario.



J. Thomas Cain

## Research seeks to integrate neural networks, knowledge-based systems

Carnegie Group has been awarded a \$225,000 grant from the National Science Foundation for the second phase of a study examining the integration of neural network and knowledge-based diagnostic system technologies into a single software technology.

The proposed work will investigate a hybrid system in which neural networks would perform an initial diagnosis via acoustic signal recognition of changes in patterns, and a knowledge-based system would perform follow-up tests leading to a specific diagnosis and repair strategy. The hybrid technology would be used to build software systems that do not require human operators for use in hazardous tasks and for situations where signal data and symbolic data must be used together for a definitive diagnosis and repair procedure.

When complete, the technology could form the foundation for prognostics, or predictive maintenance, in which a machine's deviation from correct behavior would be detected before it failed.

Vibration, acoustic, thermal, and electrical patterns change as a machine deviates from correct performance. With a hybrid system "trained" to recognize the waveforms of correct behavior, deviations could be passed to the knowledge-based diagnostic systems to begin troubleshooting.

The system might be used to develop applications in automotive, discrete manufacturing, defense, and metals industries, where early detection and repair could lead to significant savings in parts and downtime.

The first phase of the research, funded by an initial NSF grant, concentrated on integrating Nestor's NLS neural network software with Test Bench, Carnegie Group's shell for building and deploying knowledge-based diagnostic systems. Results showed that a standard low-cost platform could support a hybrid of neural network, knowledge-based system, and data acquisition software, Carnegie Group reported.

## OCR prototype scores high even with poorly written characters

Researchers at Toshiba's Systems and Software Engineering Laboratory have developed a prototype optical character reader that reportedly can recognize handwritten digits and Japanese katakana characters with an average precision of 95 percent, even when samples include poorly written script.

The system, which combines a conventional OCR system with neural networks developed following an analysis of 230,000 handwriting samples, runs on Toshiba's AS4000 engineering workstation.

First, conventional OCR techniques are used on scanned input to calculate the similarities of each character to the ideal

pattern stored in memory. Characters that cannot be clearly identified with this method are then analyzed by the neural network, which stores data on 19 groups of katakana and digits classified according to similarity. The neural network assigns the character in question to a group and then matches it to the known character in the group having the most points of resemblance.

Toshiba researchers plan to achieve even greater accuracy by incorporating additional technologies, including artificial intelligence algorithms that would help identify individual characters from the context of a phrase or sentence. The firm expects to commercialize the improved system within five years.

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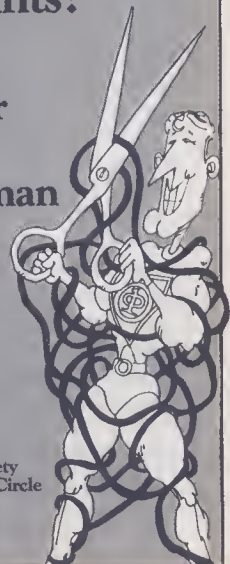
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# PRODUCT REVIEWS

Editor: Richard Eckhouse, UMASS-Boston, Harbor Campus, Boston, MA 02125, Compmail, r. eckhouse; Bitnet, eckhouse@cs.umbsky.

## Experiment design

*Daniel McAuliffe and Clifford Hamel*

Although American industry entertains the concept of statistical quality control, it has actually produced few practical implementations of this concept. The Japanese, however, have mastered the subject and enjoy an enviable reputation for producing products whose names are often synonymous with quality. The American industrial community must find a way to implement practical systems for establishing product quality and maintaining that standard. The general concepts used in experiment design can go a long way to help establish and maintain a desired level of quality.

Experiment design generally addresses the problem of finding those input values that optimize one or more outputs of a given function while minimizing the effort of finding the input values. For in-

stance, if you are developing a manufacturing tool for the infamous widget, you would want to know the tool settings that produce the strongest widget. (However, you would not want to test the tool at every conceivable combination of settings.) You would also want to maximize the yield of widgets. In this case, the desired inputs are the optimum tool settings, while the outputs to be optimized are widget strength and process yield. In the terminology of experiment design, the input variables are called factors, the values associated with a variable are known as levels, and the outputs are called responses.

Most experiment design is steeped in statistical jargon, making it very difficult for a user without a statistics background to understand the basic concepts. This is

unfortunate, since those individuals who can make the strongest use of experiment design techniques are often engineering and manufacturing personnel who do not have the necessary statistical knowledge. They need strong support from a professional statistician as well as extensive training in the practical use of experiment design concepts.

Some of the software packages reviewed do an excellent job of hiding the technical details of experiment design, which lets the user concentrate on the problem of interest and minimizes the need for strong statistical support. We strongly prefer these packages because they place experiment design in the hands of those who can make the most impact.

## Design-Ease

This package from Stat-Ease Inc. offers a basic set of two-level factorial and fractional factorial designs along with the series of Plackett-Burman screening designs. The program is driven from a main menu with a variable number of selections, depending on the state of the design you are creating or using. When the program is first invoked, seven separate selections appear, including a help entry, a configuration item for tailoring the look and feel of Design-Ease, and the Exit key.

Because there is no context-sensitive help, you must consult the main menu. The help screens describe special program keys and offer suggestions on how to order the events in designing an experiment, collect the data, and analyze the results. The manual offers much more detailed and easy-to-follow instructions than this limited menu.

The Factorial Design menu item initially selects a design from a two-dimensional table of available factorial designs. To use the table you need to know the number of factors and experiments in the design you are prepared to run. The number of variables can range between three and seven, with the number of experiments equal to either 8, 16, 32, or 64. You select the appropriate design by using arrow keys to position a highlighted block at the intersection of the desired number of variables and experiments. Pressing the Enter key displays a description of the selected design.

The Control-Enter key verifies your acceptance of the design. You are then prompted for the number of center points you wish to run. When you enter zero, you are asked for the number of blocks in the design. When you enter a nonzero value for the number of center points, no

prompt appears because the software does not permit using blocks together with center points.

The F3 key selects the Plackett-Burman design option. Designers generally employ these designs for screening several variables with a limited number of experiments. You select a design from a simple menu containing a list of variable ranges and the number of associated experiments. You must enter the actual number of variables you will be using. Design-Ease then generates the appropriate Plackett-Burman design.

Once you have selected a design, the number of entries on the main menu expands to include choices for

- entering the names of variables and responses,
- entering variable limits,
- entering response values,

- performing data analysis, and
- creating reports.

In the natural sequence of events, you enter the variable and response names and variable limits after you choose the design. You can then print a copy of the design that lists the experiments in run order, perform the experiments, and enter the response values. Design-Ease lets you block experiments in case you can't perform all of them at one time. The response entry form displays up to 16 observations of three responses at a time. Design-Ease verifies that response values are numeric at the time of entry. Because the data analysis can't be performed if any data is missing, you must enter all required responses. Design-Ease also lets you read data from a file.

Design-Ease does an excellent job of performing basic data analysis, which includes transformation of response values, computation of effects, plotting of effects, analysis of variance (Anova), and the analysis of residual values.

All graphs are immediately displayed in graphics mode when they are created, but reports are stored in a memory buffer. As you create more reports, they are appended to the buffer, which acts somewhat like a queue and deletes old information to make room for new. The contents of the buffer are available for

viewing at any time and can be erased or printed to a permanent disk file.

Design-Ease performs all analysis on one response at the same time. When you have selected a response, you can elect to transform the response values using a wide range of available functions including square root, natural log, inverse, and power. Normal and half-normal probability plots can then be used to determine those values with significant effects. Design-Ease attempts to fit a line to the set of response values. You can then interactively move the line around the screen to position it. You can also tag outlying or other points for inclusion in the final model. Further analysis is performed using the set of selected points. Single factor plots, plots of two-factor interactions, and cube plots for the case of three factors are available. The cube plots are stored in the memory buffer rather than displayed immediately.

An extensive set of plots is also available for residual values. These include normal probability, residuals versus predicted values, and residuals versus run order or a variable. The plot capabilities provided by Design-Ease are intuitive, easy to use, and extremely responsive.

At any time during the creation of a design, or the analysis of the collected response values, you can view the state of the design by selecting the Design

Status entry from the main menu. This entry, which lists the actions you have performed, is very useful when you have collected a large number of designs on disk and want to know the state of each one.

The documentation provided with Design-Ease consists of a three-ring binder containing sections on setup, program usage, configuration, the statistical features of the product, and a tutorial. The statistical section is very detailed. The distribution disk contains a set of data files for the tutorial. These examples are extracted from *Statistics for Experimenters*, by G. Box, W. Hunter, and J. Hunter, John Wiley and Sons Inc., New York, 1978. Thus, you can refer to the theoretical foundation of the program.

Design-Ease is an excellent product, especially for the scientist or engineer who is new to the subject. It provides most of the features you will encounter when you are first introduced to the subject, without bogging you down with statistical jargon. We highly recommended it as a starting tool for creating and analyzing experiment designs.

Design-Ease is available for \$300 from Stat-Ease Inc., 2021 E. Hennepin Ave, No. 191, Minneapolis, MN 55413.

**Reader Service 21**

## Design-Expert

Design-Expert, Version 2.0 (also from Stat-Ease), extends the domain of designs from the two-level factorial and fractional factorial categories into the area of response surface designs and mixture experiments. The program lets you optimize the results of your analysis, including several responses at once.

The general appearance and operation of Design-Expert is almost identical to that of Design-Ease. The program uses the same menu style with a variable number of items, depending on the state of the design and analysis you are performing. The main menu initially includes selections for program configuration, design selection, and utilities.

The configuration menu item is more extensive than that found in Design-Ease. You can select the graphics adapter, adjust the size of the overlay buffer to improve program performance, and specify the type of printer you have installed and the control strings used with the printer. You also have limited control over the format of the reports printed by Design-Expert, such as the number of

lines per page and the number of characters per column. The package also supports the Lotus-Intel-Microsoft (LIM) expanded memory specification (EMS).

The Design Selection item on the main menu lets you choose either a mixture of designs or a response surface design. Since the program flow is very similar for both, we concentrate here on describing a program when a response surface design is selected. Once you select the design type, you can choose from two to six variables by positioning a highlight bar on the desired number in the Number of Variables menu. You then choose the response surface design type from a fixed list consisting of these selections: central composite, Box-Behnken, and full factorial. Design-Expert determines the number of trials from the design type and the number of variables. You can then split them into blocks to ease data collection.

Block sizes are chosen from a predefined list. You can specify an alpha value for a central composite design. This parameter is the distance from the

axial points of the design to the center of the factorial. After you select these parameters, you are presented with a variable definition screen. You must enter the name, unit of measure, and lower and upper factorial levels. Pressing the F3 key at this point fixes the design and returns you to the main menu. You must be sure to save the design in a disk file before continuing or you will lose the work you have just created.

Two new entries now appear on the main menu, one for design editing and one for response editing. The design editor lets you view your design in either coded or uncoded form. In either case the listing displays the trials in the randomized order in which they are to be run. At this point you can replicate a trial by simply positioning the cursor on the desired trial with the arrow keys and pressing the F2 key. You can also specify the block in which you want the replicated trail to appear and rerandomize the run order either within a block or for all blocks. Once you are satisfied with the information on the design editor form,

you can print a copy of the form from within the Utilities menu, conduct each experiment, and record the response data on the form. The form prints in run order for ease of recording.

The response editor format is identical to that of the design editor, except that it does not let you change the process variable information. The format also lists the trials in run order. You are provided space for entering the response names and the values of each response collected during the experiment. You can also load response data from an ASCII data file.

Once you have entered the response data, you are ready to perform the analysis. Design-Expert inserts additional items in the main menu for this purpose of data analysis and optimization. The first step in the analysis is to compute all effects in the design. You then choose the maximum degree of the polynomial you want to fit to the data, either linear, quadratic, or cubic, and perform any desired transformations on the response data. The list of available transformations is very similar to that of Design-Ease.

After you select the appropriate transformation, the program begins the calculation phase and places the results in a memory buffer that you can view, modify, save to a disk file, or print. If you chose a quadratic polynomial for fitting the data, the buffer contains Anova results for both the linear and quadratic model, as well as a summary table. The table shows the significance of those terms added when a polynomial of higher degree is used and also includes a lack-of-fit table to compare the residual error with the pure error due to replication. Given this information, you can choose an appropriate model and examine various additional statistics related to it (such

as tests) to determine the significance of each model coefficient and the analysis of residual values.

Design-Expert provides a set of plots very similar to those found in Design-Ease. These include the normal probability plot of residuals, plots of residuals versus predicated response values, residuals versus run order, and residuals versus a specific variable. In addition, contour plots can be generated for the response surface for any single response in the design. Since these plots are two-dimensional, you must specify which variables define the axis and the minimum and maximum values of the variables. If you have more than two variables in a design, the value for each additional variable is held at a constant level specified by you at the time you choose the primary axes variables.

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### **Design-Expert is an excellent tool for performing simple, basic response surface analysis.**

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Design-Expert picks five different levels between the variable minimum and maximum and partitions the axes accordingly. It also picks five contours between the minimum and maximum values of the response as defaults and displays the contour lines for each value. You can select new contour levels for the response and regenerate the plot until you have fully explored the response surface.

If you are dealing with multiple responses, Design-Expert lets you determine the regions in which two or more responses simultaneously meet desired criteria. You can superimpose response contours and visually examine the resultant plot. Before you can perform the optimization process, you must first model each of the responses and perform any necessary transformations. You are then presented with an Optimization Response Selection form. You must enter the type of model on the form, along with the lower and upper specification limits if you so desire; otherwise you may leave the limits open-ended. Design-Expert plots the contour, proceeding as if it were plotting a single response. However, those areas in which all specifications are simultaneously satisfied are left blank, and those in which any one specification is met are shaded to reveal the desired area.

Design-Expert is an excellent tool for performing simple, basic response surface analysis and analysis of mixture designs. It requires little learning time, has consistent menus, and performs calculations very responsively. However, the data analysis features require a better-than-average knowledge of statistics or at least some assistance from a professional statistician. The combined single copy price of Design-Ease and Design-Expert is \$995, a substantial investment. Since so many of the features of the two programs are identical, it would seem appropriate to combine the two programs to provide some significant savings to the user.

Design-Expert is available for \$695 from Stat-Ease Inc., 2021 E. Hennepin Ave., No. 191, Minneapolis, MN 55413.

**Reader Service 22**

## **Xstat**

This remarkable program has many exceptional capabilities in the field of experiment design. The program comes on two 5.25-inch disks and operates on any IBM PC or compatible with a minimum of 256 Kbytes of memory.

Options include nearly all known classical experiment designs. You can even input your own unique design. However, the manual clearly points out that Xstat is not designed for "massaging massive amounts of happenstance data."

The brief instructions included with the program are easy to understand. You can operate the program from a floppy or hard disk. Input can occur through the keyboard, from a file, or even through

one of the communications ports. First-time users of Xstat can employ the menu structure for operations until they become familiar with command syntax. Then they can turn the menus off.

The well-written manual lists commands in alphabetical order with explanations and examples. The manual and disk contain 10 examples to help you review the program options and capabilities.

Xstat's nonintuitive menus do not lead you from the beginning of the experiment design to the final analysis. The program assumes that you have the background necessary to understand what must be done. If you do, the menus pro-

vide sufficient information to use the available options.

For example, when you have defined the independent variable names and their ranges, you select the design option. A menu then displays all possible designs, whether Box-Wilson, Mclean-Anderson mixture, or factorial. In each case, the proper number of trials can be selected based on the number of independent variables. The program checks for errors at each step to ensure the input is consistent with previous design constraints and requirements.

The program also writes screen output to memory and lets you view it at any time by pressing the F10 key. You can

also select sections of this memory to send to a file, printer, or serial port. Extended sessions of Xstat take up large areas of memory and exiting the program is the only method of releasing the memory. You may then restart the program and continue where you left off. Output during program operation can also be routed to a file, printer, or serial port.

At any time, you can print out a work sheet of the experiment design with space for logging the response levels for each trial. Once the response levels have been input, either manually or from a file, you can print a summary of the design with the associated responses to either a file or printer.

The analysis of your data may include residuals analysis, analysis of variance, or tests of regression. You use simple X-Y or contour plots for responses and view them on any screen, even in non-graphics mode.

A feature of the contour plotting routine lets you request a plot of every pos-

sible combination of the variables over a given range. Those variables that are not part of the contour plot may be set to any level you select. A key option of the contour plotting is superimposing two responses on the same graph. This is very useful when it is important to understand the effects of variable level changes relative to two simultaneous responses. For example, you can plot the effects of time and pressure with product yield and cost to understand how changes in yield affected cost.

One of the most powerful, important functions of Xstat is optimizing a process. You can find the combination of variable settings that maximizes or minimizes one response while restricting other responses to certain regions of interest. This option simplifies the optimization of a process for one or more responses, making it cost effective. You can save the optimum settings and use them in the contour plotting routine to inspect the response levels.

Xstat is an exceptional program, provided you have sufficient background. This well-written package can more than handle any requirement for the design and analysis of experiments and can help you greatly to optimize processes. Although you will need to invest considerable time to understand the program's command structure, it is definitely worth the effort.

The suggested retail price for the package is \$350. Minimum system requirements include an IBM PC AT or XT or equivalent, two disk drives, a monochrome monitor, and PC DOS 2.0 or higher. (For best performance, add memory and a math coprocessor.)

For more information, readers can contact Wiley Professional Software, John Wiley and Sons Inc., 605 Third Avenue, New York, NY 10158.

**Reader Service 23**

## Echip

You can run Echip from the command-line mode or a series of interactive menus. The novice user will probably want to use the menu system, since it is much easier to follow the general course of progression through a design when the menus are present.

The menu tree follows the flow of the normal design process. The main menu contains entries for determining resolving power to test the feasibility of a design, creating the design, entering response values, analyzing the data using regression analysis, and displaying contour plots. Each submenu contains more menus, but they are well structured and relatively easy to traverse.

Although context-sensitive help is available throughout the menu tree, a no-help message often appears (as in the case of the Standard Designs entry in the Design menu). When help messages are available, they are generally complete extractions from the course text manual. The F2 key is reserved for displaying help on the use of the keys themselves.

A number of standard designs are available with Echip: linear, linear with center point, Plackett-Burman, factorial, quadratic, central composite in a cube, central composite in a sphere, and cubic. You select the designs from the Design menu and depress the F3 key to generate them.

Data entry is one of the major weak points in Echip. The user enters virtually all data through a pop-up window with a

text editor. The data fields are not edited at the time of entry, so errors usually don't show up until the data is actually used. For example, users enter variable names together with low and high limits by means of the editor and then use the names when a design is generated. When an error — such as a comma between fields — occurs, a rather meaningless error message (such as "expected space 1, 2") appears during the attempt to create the design. This can create a lot of confusion and unnecessary searches for sources of error. Errors in data entry are best handled at the time of initial entry.

The major emphasis in Echip — and its strongest feature — is producing a variety of contour plots. Response surfaces with three or fewer variables are readily analyzed with either two- or three-dimensional plots. Two-dimensional plots are available in both character and graphics mode. Actually, you can use plots for any number of variables. In this case, the plot displays the fixed values of the off-axis variables.

You select the contour option from the main menu. You can specify the variables that appear on the abscissa and ordinate. Other features include interval spacing on the axes, plot size, and whether the intersection of the convex hull of the data and the contour plot plane displays as a mark on the screen. A convex hull represents the region in which a data set is defined. It consists of the set of all data points together with the

set of all points that are the weighted averages of the data, with the weights summing to unity. The F3 key displays the two-dimensional character plot. At this point, you can switch to either a two- or three-dimensional graphics plot by using the F8 and F9 keys. You don't need the contour menu. The delay between your request and the time a graphics plot appears on the screen can be very long, especially with three-dimensional plots. Because the screen is blanked out during this time, the system appears to be hung up. The designers would do well to display some type of message to indicate that the program is working.

A mouse allows you to make full use of the contour plots. You can display and print plots without a mouse, but you can't manipulate them. The mouse buttons increase or decrease the values of a data field and update the graphics display. When the mouse cursor is positioned on the plot surface, the value of the response surface displays in a box at the lower right-hand corner of the screen. The 95 percent confidence limits, an indication of the accuracy of the response value, are also displayed along with the value. As you move the cursor across the surface, the response value and limits change.

The amount and type of information that appear on the screen along with the contour plot depend on the type of plot you have selected. The symbols used in a character plot are defined in a column to

the right of the plot. The value of each off-axis variable is always present and can be increased or decreased by clicking with the left or right mouse button. Double-clicking the left button updates the plot. Using the End key and entering the desired value sets a specific value for an off-axis variable.

The F3 and F4 keys alter the type of data appearing in the information box in the lower right-hand corner. The F3 key changes the display to row number, data value, and standard deviation, while the F4 key causes the row number, influence, and residual value to appear. The name of the response associated with the plot appears in the upper right-hand corner. Clicking on the name changes it to another response, highlighted in bright white to indicate that it is not related to the plot being displayed. Double-clicking on the name updates the plot.

A warning message appears when you are outside the convex hull. The F1 key brings up a help screen, and the F2 key cycles through a display of the key definitions. These appear in a single-line window on the bottom of the screen with a maximum of three definitions appearing at once. A single window that shows all definitions simultaneously would be much clearer. The character plot responds best in terms of screen-update time when you move the cursor across the plot.

The data appearing on the screen for

two-dimensional graphics plots resembles that displayed for character plots. The response name field and the information box in the lower right-hand corner are treated in much the same way. However, you can't enter specific values for an off-axis variable unless you switch to the character plot display, enter the value, and switch back to the graphics mode. Although the values can still be altered in graphics mode with the mouse buttons, they change by a fixed amount (20 percent) with each click.

The three-dimensional contour plot is similar in functionality to the two-dimensional variety except that moving the cursor across the plot does not show the values of the response variable, nor does clicking on the axis shift the plot along its length. You can, however, rotate a three-dimensional plot through a change in either azimuth or elevation, or both. The current value of each angle displays in a separate box in the lower left-hand corner.

Clicking inside the boxes and double-clicking to update the plot changes the angles. We found this feature to have limited value. Unless you have an exceptional sense of spatial visualization, it is extremely difficult to follow changes in attitude, especially when they occur in large increments. In addition, the plot update takes so long that we felt more frustration than insight into the problem.

Contour plots can be printed on a

number of devices. Echip supports three parallel ports and a serial port. Any plotter that supports the Hewlett-Packard Graphics Language command set can also be used. Plots can be output to a disk file in TIFF (Tagged Information File Format), a popular graphics interchange format; EPS (Encapsulated Postscript); and HPGL. If you have a word processor that supports any of these formats, you can include the contour plots in your reports and presentations.

The documentation package provided with Echip consists of a users manual and a supplement for version 5.0. The manual contains a course text, an advanced course text, a description of the menu system, material on program documentation, and a technical supplement. There is no reference manual. Echip contains a number of predefined experiments that can be used with the course text. Although the manuals are generally well-done, some terms are unclear.

Echip can be a valuable tool, especially if you are interested in using contour plots. However, it does have a number of weak points in data entry and editing and requires a great deal of response time to update contour plots in graphics mode.

Echip Inc. is located at 7460 Lancaster Pike, Hockessin, DE 19707. A one-year license costs \$1,495 (a \$150 yearly renewal fee includes updates).

**Reader Service 24**

## Taguchi Analyst

As the name implies, this Texas Instruments package facilitates experiment design and analysis using the Taguchi method. The program emphasizes letting the user concentrate on the experiment rather than how to determine the design. Step-by-step on-screen instructions guide you through a series of panels that require some form of input or action before proceeding to the next panel. The objective of the panels is to help you organize, plan, and analyze your experiment. Most panels have help key information to provide additional descriptions of the required input.

One of the most interesting and useful parts of the program is the Process Definition option. Parameters that might have an effect on the evaluation are entered in this section, including those parameters used to gauge the quality of evaluation. At this point, you also define the possible ranges or levels that each variable or quality characteristic might have. These variables provide a basic understanding of parameters that might affect the pro-

cess or tool under evaluation. This brainstorming session is a very important part of the Taguchi methodology.

Next you use the Planning and Design option to select the variables that you want to use in the experiment. If a variable or quality measurement characteristic was not defined in the brainstorming section of the program, you must go back to that section and enter it. Although this seems like a duplication of effort, remember that the first session was to lay out "all" parameters that could affect the process and in this section you are defining only those variables that will be tested in the evaluation. This sequence of events is quite helpful for those who are not familiar with experiment design but is a bit of a bother for experienced users. Two or three levels of each variable may be defined for the inner array and only two levels for the outer, or noise array. You can also define the interaction of any two variables and the number of replicates and repetitions at this time.

This section prints out forms for sum-

mary, description, and array files. The summary file presents the experiment name, participants, department, file names, and goals. The description file lists the variables under investigation and their levels, while the array file presents the Taguchi orthogonal table used in the evaluation. A cost estimation selection lets you define the actual cost of each experiment as well as the total for the evaluation.

One useful option allows you to rearrange the column location of the variables to determine possible interactions. At any time, you may return to the Planning and Design option to design another experiment using a different combination of the variables from the brainstorming section. Each iteration of this section creates another experiment file.

To obtain a printout of the data-collection sheets, you must return to the second main menu and select from a utilities option. The DOS PRINT.COM option must be loaded. Note that this option produces large quantities of printed material; one

sheet per trial is typical.

The data-entry option is quite confusing. We expected to find a separate option for data entry instead of View Data, Edit Data and Print. The view mode scrolls through data already entered, and the edit mode is for the actual data entry. Data is manually entered using the Edit option one trial at a time, and each trial condition is identified to help determine where the data should go. Actual input of the data is reasonable, with good layout and description for each input field. Error checking occurs at each field to ensure the correct values. You should use

the data-collection sheets to input the data because they help identify the proper row and column for each input. With some experiments that have a hundred or more tests, this could prove quite confusing.

Analysis of the results is straightforward but limited. The program presents a set of solutions or estimates for the best operating conditions for the variables and quality characteristics. For each response you can view Taguchi's signal-to-noise level analysis or the process averages. Anova tables are also available for each of these. The program performs cal-

culations automatically.

Taguchi Analyst is useful in the preparation and design of Taguchi orthogonal designs. Its strongest points are in the actual preparation for the designs, while its weakest points are in the presentation of these designs and analytical results.

Taguchi Analyst is available for \$1,495 from Texas Instruments, PO Drawer 1255, Erwin Highway, M/S 3524, Johnson City, TN 37605-1255; (800) 284-9084.

**Reader Service 25**

## Statgraphics

This powerful general-purpose statistical analysis package from STSC Inc. strongly emphasizes the graphical representation of problem data. The system can perform a variety of frequency tabulations, Anova, regression analysis, time series analysis, multivariate analysis, and two- and three-dimensional plots. The explicit experiment design features of Statgraphics occupy only a small portion of the overall capabilities of the system, although many of the separate analytical tools can be used to study the results of an experiment. Full and fractional factorial designs are available, along with central composite designs, a feature called alias structuring, and response surface plotting.

Factorial designs consist of two-level experiments with a maximum of 11 factors, 128 runs, and either one, two, or four blocks. You build a factorial design by selecting the Experiment Design item from the main menu and then choosing the Full and Fractional Factorials entry on the secondary menu. The input screen contains entry fields for the number of blocks, factors, and runs. Once these items are entered, the appropriate design matrix appears with additional columns for the run number, block number, and response values. The design matrix displays with a minus sign to represent the lower level and a plus sign to represent the upper level of a factor.

There is no provision for giving names to the different variables, entering the ac-

tual minimum and maximum values of the variables, or dealing with more than one response at a time. This often makes the work sheets difficult to follow. Once you have created a design, you can use the F5 key to call up a menu of options to deal with it. The options include selections for randomizing the run order, entering the response data, estimating the main and interaction effects, generating a normal probability plot, and saving the design and estimated effects.

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**Once you have created a design, you can use the F5 key to call up a menu of options to deal with it.**

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The Central Composite Designs option generates a design matrix for a second-order central composite design with a maximum of eight factors. After selecting a design, you must save it to disk. You can't enter response data from a separate options menu. You must use the system multiple regression procedures to analyze the results of the experiment.

The Alias Structure procedure generates a matrix of correlation coefficients

between the main and interaction effects. The design matrix can come from the Full and Fractional Factorials option, the Central Composite Designs option, or your own creation.

The Response Surface Plotting option generates contour and three-dimensional plots of second-order polynomial functions. You can plot an X-Y polynomial, a matrix of input values, or a user-defined function. You can enter the coefficients of a general second-order polynomial in two variables and plot a user function with a valid Statgraphics expression. The expression can be constructed from operators that range from simple arithmetic to functions such as square root, logarithmic, and exponential. The operands in most cases can be scalars, vectors, or matrices. The well-constructed response surface plots display quickly and are easy to read.

Statgraphics is a powerful, flexible statistical tool for analyzing data with a wide range of methods. If you are looking for a general statistical package that contains some experiment design features, we recommend it highly. However, if your main interest is in the generation and analysis of experiment designs, better options are available.

STSC Inc. is located at 2115 E. Jefferson St., Rockville, MD 20852; (301) 984-5000. The suggested retail price for Statgraphics is \$895.

**Reader Service 26**

## Statistical programs

Occasionally a program appears that presents an old subject in a completely new way. Statistical Programs of Houston, Texas, has done a remarkable job

with Experimental Design. This expert system determines which experiment design is most likely to meet your needs. It does this by asking a long series of ques-

tions about experiment design.

The questions make you aware of the same important aspects of experiment design that a consultant would normally

consider. Some of the topics presented relate to

- the number of variables,
- the possible presence of interactions, cost, or time required for the experiments,
- the types of responses to be measured, and
- whether the goal of the experiment is to fit a response surface.

If you are unsure of a particular answer, you can assign a confidence factor to your response ranging from 0 to 100 percent.

At any point in the program when you are unsure of why the question is being asked, simply press the appropriate key and a small window pops up to give an explanation. If you need more help in understanding the terminology, press another key to review one or more descriptions of the terms. Statistical terms that have associated help screens are highlighted.

At any time during the session, you can exit the program to return at a later time or review and update an earlier question. A status report is also available at any time. This report lists 17 designs, ranked according to your needs. (You may review the evidence that led the program to rank the design at that level.)

Another interesting aspect of the program is the extensive list of references. For each type of experiment design, you can review specific reference books for more information. In most cases, the reference includes page numbers.

The program recommends the type of design to use. However, it neither generates those designs nor performs any data analysis.

Statistical Programs also offers several other products that can be used for the design and analysis of experiments, including Screen and Factorial-Design. Because each program is purchased separately, users can set up their own series of specialized programs for process or tool optimization.

Screen is a simple but powerful program for the design and analysis of screening experiments. After selecting an experiment file, you input a low and high level for each factor to be tested, up to

35 factors. The design is defined by the program. You can choose a fold-over design if your design is saturated. You may indicate the complete design to be replicated or one particular point in all designs. Work sheets for each trial can print to disk or a printer for use in recording pertinent data during the experiment.

After designing the experiment, you can also input up to eight responses to be measured. Response data is input by keyboard only; no transformations of data are possible. You can review and revise the response data at any time.

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### **At any time during the session, you can exit the program to return at a later time or review and update an earlier question.**

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The program automatically analyzes the screening experiment and prints it to a file or printer. The analysis of the experiment design is in the form of the mean of the effects.

Screen presents its data analysis in two forms. The first form is the average effect and mean square relative to each factor of the experiment. The results are ranked relative to their importance for each factor to help you understand which factor has the greatest effect. In the alternative form, the effects of the factors upon each response are ranked according to the responses. This helps you understand which response is most affected by the factors in the experiment.

Factorial-Design, the third program in the series, may be used after the screening experiments have been completed to help optimize a process or tool. Depending upon the number of factors to be tested, you begin an experiment design by entering the program name FACTOR2, FACTOR3, or FACTOR4.

Variable names for the design must start with the letter *x* to be valid. Defini-

tion of the design conditions are not as simple as in the Screen program. One must have a more thorough understanding of experiment design concepts to use the program.

You can print work sheets for the experiment to file or disk. You can only input response data through the keyboard, but you can change it at any time. Only one response may be optimized for each experiment. Analysis of the response data is also not very intuitive and requires that you have knowledge of experiment analysis concepts. Analysis options include response equation coefficients with confidence limits, residuals analysis, Anova, the option to alter the model, and most importantly, contour plots. All analysis may be output to printer or file.

The Experimental Design program is a very useful tool. It will definitely help you understand more about your experiment design and provide valuable information about the design of experiments. The subject references and descriptions are especially interesting. The Screen program is a worthwhile for beginners and experts for the design and analysis of screening experiments. It is simple and easy to run. The only drawback to the program is the extensive use of exponential notation, which makes interpreting the analysis difficult.

Factorial-Design valiantly attempts to automate the process optimization problem, but it lacks many user-friendly concepts found in the other two programs. Exponential notation on printed output causes confusion. The requirement that factor names start with an *x* also makes the program difficult to use. In general, it's not as easy and straightforward as the Screen program to use, both in the design and analysis of the results. The capability to handle only one response limits program usefulness.

Experimental Design, Screen, and Factorial-Design are available from Statistical Programs, 9941 Rowlett, Suite 6, Houston, TX 77075; (713) 947-1551. The retail price for each is \$295.

**Reader Service 27**

## **Summary**

The experiment software reviewed here offers a wide range of capabilities, from the basic design choices found in Design-Ease to the more sophisticated design and analysis features found in

Echip and Statgraphics. You probably can use the more basic packages with little training or assistance from a statistician, but the more advanced packages may require extensive training and heavy

utilization of the services of a resident or consultant statistician. In either case, the potential for substantial process improvement using one of these packages is well worth the effort.

## Review notes

**Easiest.** About 10 years ago, I was using a Minc system from Digital Equipment Corp. for gathering and analyzing laboratory data. This system, based on a cart-mounted mini-computer with limited disk space and low-resolution black-and-white graphics, was a good forerunner to today's PC-based system, which is considerably cheaper, smaller, and more versatile. DEC sold a complete solution at the time — both the hardware and the software. Today, with the large number of PC and data-acquisition board manufacturers, the solution is to find the right software.

A number of software vendors offers data acquisition, analysis, and graphics software all rolled into one convenient package. Frankly, they are all pretty good, and some have been around for a few years. But one stands out because it is from the same company that produces Asyst (see *Computer*, June 1990, p. 104) and offers not only the features that you need to get started but an upward migration path to a more powerful system. The product I'm talking about is Easiest from Asyst Software Technologies.

To understand why the vendor named this product Easiest, refer to the figure. This screen is filled with numerous icons to determine:

- what data is to be gathered,
- where it is to be stored,
- how it is to be processed, and
- how it is to be displayed.

The acquisition icons at the left of the screen offer A/D acquisition (into a memory array or a disk file), D/A output, digital I/O, and closed loop control (PID, or Proportional Integral Derivative). A keystroke, timed delay, rising or falling edge, digital line, or an external source can serve as an acquisition trigger.

The memory icons just to the right of these icons specify the memory arrays, one for each channel. Below them are the icons for copying data between memory locations (including a temporary location) and clearing the various memory locations. Below these icons are the analysis icons for processing the data. Signal analysis includes a fast Fourier transform with four window methods, and integration, differentiation, and curve fit (us-

ing up to a fifth-order polynomial). Filters include low, high, and bandpass. Arithmetic options are also available. Data can be stored in files for retrieval or transferred to Asyst (using the migration-path software, which is free to owners of both Easiest and Asyst) for subsequent analysis.

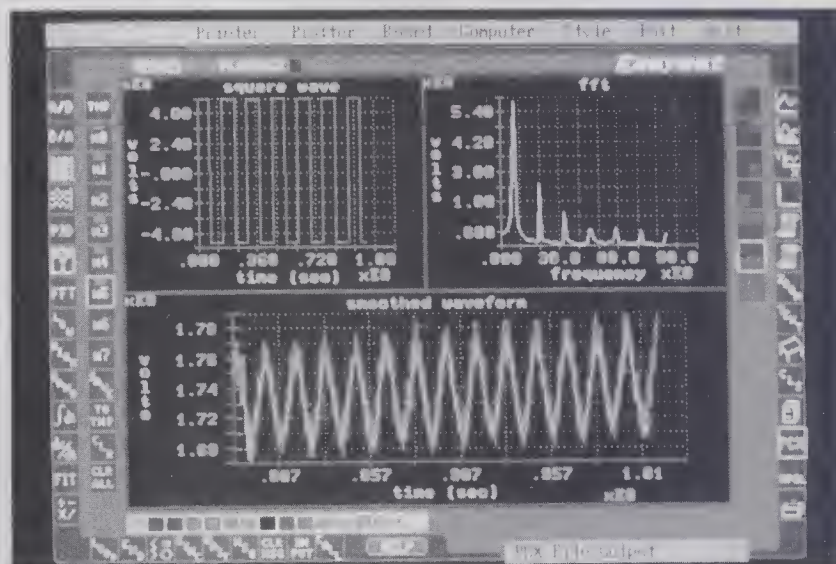
Graph area icons on the right inside of the screen let you choose between full, half, and quarter display areas. To the right of these, display icons offer data and axis plotting, labels, scrolling from memory and disk files, and zooming in on the data being displayed. Below these are the in/out icons for creating data tables, clearing the screen, performing I/O from disk files, and sending screen data to a PCX file, plotter, or printer.

Having set up a series of steps for Easiest to perform, such as the acquisition and display of data, the next step is to make up a sequence that can be executed in place of the individual steps. Along the bottom of the screen are the programming icons for just that purpose. By clicking on the record button near the top left of the screen you can record your keystrokes for subsequent playback. You can also imbed the programming steps and following sequences (up to three levels) within one another. If you make a mistake, you can invoke a text editor from the top menu line. This line also includes configuration of the channels, printer, plotter, board, and graph style.

Easiest seems well suited to the laboratory professional who wishes to gather, analyze, and display low-frequency (less than 1-kHz) signals. The system is purposely limited in terms of the size of the memory locations (1,024 samples per location), the collection rates, and the capability of simultaneously running analog signals in and out. However, since the A/D acquisition rate is set both by the maximum board rate (with DMA) and the particular processor chip or speed used in the your PC, it is possible to gather analog data and pass it on to Asyst for further processing.

For example, A/D to a file (up to 8 Mbytes worth) is rated at 45 to 65 kHz single channel using DMA. On the other hand, the Strip Chart data rate is .01 to 100 Hz per channel with concurrent display and .01 to 800 Hz without it; and the PID is rated at .01 to 5 Hz per D/A channel, while supporting real-time control of set-point, proportional, integral, and differential coefficients.

The Asyst company made the data-acquisition drivers external to the base software (whether it is Easiest or Asyst) so that you install drivers before starting up Easiest. You can simply add new drivers and upgrade older ones. A sampling of the boards currently supported includes the Analog Devices RTI-820; Burr Brown



The Easiest expert system automatically acquires and graphs data and executes the frequency analysis.

PCI-20087W and -20098C; the Data Translation DT28x series; the Keithley DAC K500/575 as well as the Metrabyte DASx series; and the Markenrich Waag. Regardless of the number of A/D channels on the board, Easyest uses only the first eight. When the data rates you select are too high, the software resets and you must start over.

I found this package to be easy to use with the graphical interface, although the interface is nonstandard (that is, SAA compliant). The convenient windowing aspect makes it easy to select among choices. However, the system only works with a mouse. Those who want to select/move between fields using the tab, space, and return keys will be disappointed.

I'd also like to see an easy way to integrate the application programs that analyze gathered data. Ideally, these programs should let users have buttons to call up the analysis routine and process the data in one of the memories. Adding statistical processing is a case in point.

The manual is only fair and would benefit from more examples, particularly for programming. Fortunately, you almost don't need the manual to use the system since each icon is explained by clicking on the right mouse button. If you forget what's going on, the currently selected command appears at the bottom of the screen.

System requirements include a PC, DOS 2.0 or higher, 555 Kbytes of available base memory (you may need to unload some TSRs), and a hard disk. Although floating-point-emulation software is supplied, it runs much faster a chip.

I found Easyest easy to use and practical. Often I need to verify that I have set up an experiment correctly before going into the full collection process. On other occasions, I want to gather some data from a device that appears to be malfunctioning so that I can examine it off line to find the problem. Easyest is well suited for these kinds of tasks. It also serves as a good front end to the Asyst package. Competitively priced with similar products, the base system sells for \$765, which includes one driver and technical support. Additional drivers are \$100 each.

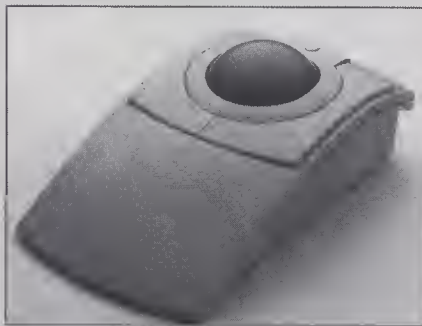
I'm glad I had a chance to evaluate the product because I have found numerous uses for it. I heartily recommend it.

Asyst Software Technologies Inc.

is located at 100 Corporate Woods, Rochester, NY 14623; (800) 348-0033, (716) 272-0070; fax (716) 272-0073.

— R. Eckhouse

#### Reader Service 28



Microspeed's PC-Trac trackball

**PC-Trac.** Several years ago I wrote about the first trackball produced by Microspeed. Fast Trap has served me well, and I am still enjoying it. However, when I saw the latest incarnation, I knew that I had to take it for a spin. The sleek, trim design of the newer PC-Trac fits my hand very well (see photo).

I think it's the only trackball that caters to the two types of trackball users—the "overs" and the "unders." You can tell which one you are by whether you place your hand completely over the roller ball and click at the top of the buttons or use your fingertips to roll the ball and click at the bottom.

You have your choice with PC-Trac because the buttons aren't really buttons but rather large, C-shaped surfaces that completely surround the roller ball, thereby allowing you to reach them from nearly any position. The one catch is that the third button is only accessible by reaching above. This is not really a limitation because most programs only require a two-button pointing device.

If you're like me, you prefer a trackball because it takes up less desk space than a mouse and doesn't require the same amount of movement. More important, because it doesn't jerk to a new position when your hand leaves it, you have a finer level of control. And when you need a "sticky" button for such operations as highlighting a sentence or erasing a large area within a picture, the drag lock feature of the third button comes in handy. The same button can also be used in chord mode (the equivalent of pushing both buttons simultaneously).

PC-Trac is fully Microsoft-Mouse compatible. I have been using it for sev-

eral months with the Windows mouse driver without a problem. Of course, if I wanted more functionality I could also use the two software drivers that come with the device.

Key Map bridges the gap to programs not designed to work with a pointing device. Precision Pointer offers more control over the trackball like x- and y-axis gain, including ballistic gain as well as the clamping value. For those unfamiliar with these terms, the gain defines how far the cursor moves in relationship to the movement of the trackball. The clamping value restricts the total number of pulses that the pointing device can send in one full movement. By the way, resolution of the PC-Trac can be set anywhere between 50 and 1,000 dpi.

The trackball comes in serial, bus, and PS/2 versions. Retail pricing is \$119, \$149, and \$119. Interestingly, the new bus version is compatible with the bus card from Microsoft and Logitech. Users can plug the trackball into either one of these cards without having to install the bus board that comes with the unit. I prefer the serial version because I can easily move it from one machine to another. Each version has some slight differences that are covered in the two-manual set, one called the *PC-Trac Owner's Guide* and the other the *Precision Pointer Software Guide*. Both manuals are thorough, covering much more than most of want to know. Topics include

- installing the trackball and optional bus card,
- installing the software,
- using pointing devices,
- using Key Map, including how to set up templates,
- special features, and
- technical information.

Some reviewers have been skeptical of trackballs because they think they are hard to use and usually break down. My experience is quite the opposite. I took my first unit out of the box, plugged it in, and started using it immediately (without referring to the manuals). This "must have" item comes strongly recommended.

Readers may contact Microspeed Inc., 44000 Old Warm Springs Blvd., Fremont, CA 94538; (415) 490-1403, fax (415) 490-1665.

— R. Eckhouse

#### Reader Service 29



# DCC'91

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The 44 scheduled technical talks of DCC'91 will provide an international forum for current data compression research, covering a wide range of topics including *lossless compression, image compression and quantization, fractal, transform, and wavelet techniques, source coding theory, fast algorithms, compression standards, hardware, and applications*. In addition, the 50 scheduled presentations of the conference poster session will provide attendees a unique opportunity to exchange ideas.

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## Computers for medicine

### Molecular modules run on the RS/6000

Chem-X molecular modeling software now runs on IBM RS/6000 workstations and compute servers to offer chemists 3D database building and quantum mechanics calculations. Graphics support small molecule studies. The software from Chemical Design also runs on VAXstations, Apple Macintosh IIs, and IBM PCs.

The RS/6000 outperforms other machines in terms of conformational analysis calculations, according to the company.

Researchers use Chem-X to develop new items in the pharmaceutical and protein engineering fields, among others.

An entry-level single-user license costs \$8,000 for industrials.

**Reader Service 35**

### Cray Research supports R&D in molecular sciences

The Unichem software environment runs on Cray Research computer systems and concentrates on the molecular quantum mechanical calculations that support detailed simulations in molecular and materials sciences. The package — developed with Du Pont and Eli Lilly and Company — offers various levels of chemical accuracy based on semiempirical, density functional, and ab initio methods. Users can directly manipulate the graphical interface.

Unichem distributes complex equations to Crays running Unicos Version 5.1, while the Iris workstation manages

the user interface. Users can build or import molecular structures, choose a computational method and select its parameters, control computations, and visualize results. These visualizations are

uniform for each application program.

The company plans to ship the package in April 1991.

**Reader Service 36**

### Toshiba enhances workstation

The SE Workstation processes 3D images for use in conjunction with MRI (magnetic resonance imaging) scanners. Introduced in November 1989, the workstation allows technologists to view and manipulate MRI data on brain, spine, and bones without preprocessing.

Users can now increase slice thickness to improve signal-to-noise ratios. Stereo-pair generation provides two identical images adjusted at specific

angles for improved visualization. The workstation automatically generates radial oblique views. Intelligent magnification supports comparative studies.

The enhanced version of the 900-MIPS workstation comes as an option to Toshiba's MRT-35 midfield system and the Access permanent magnet system. Options for the MRT-150A and MRT-50 units will ship in mid-1991.

**Reader Service 37**



The interactive SE Workstation accompanies MRI scanners and uses a mouse-driven interface.

## Medical records linked to doctor's office

The Medical Manager Version 7.0 from Systems Plus lets physicians upload and download clinical information to and from hospital and laboratory sources. A Data Merge enhancement customizes procedures and sends information to other software packages. Data can fall into 99 clinical history categories.

Physicians can also automate billing and insurance information and appointment schedules.

The system runs under DOS, CCI Concurrent DOS, Unix/Xenix, and network environments on IBM 6000s, PS/2s, NCR Towers, and HP 9000s, among others.

**Reader Service 38**

## Terminal doubles X Window display

Jupiter Systems dual-display 256-color X terminal for medical imaging supports two 19-inch, 1,280 x 1,024 monitors. Model 412 features include zooming, support of 12-bit image data, memory expansion to 16 Mbytes, and arithmetic picture options. The monitors feature an Invar shadow mask that focuses dynamically and an antireflective coating to enhance contrast.

When the user moves the mouse-driven cursor off the boundary of one display, it immediately appears on the other. Each display controller has its own color look-up table and graphics accelerator.

Model 412 uses a 25-MHz 68030 CPU. X11 release 4 server software supports X Windows, including X display manager control protocol, Shape for nonrectangular windows, and Telnet.

**Reader Service 39**

## Image processing on a Macintosh

IP Lab Spectrum-364 from Signal Analytics provides a number of image-processing operations for such applications as biology and medicine. These include point functions, linear filtering, morphology, fast Fourier and cosine transforms, and automatic and manual measurements and binary operations.

Users can apply these operations to defined regions of interest and obtain statistical analyses on arbitrary polygonal regions. These image-processing functions can also be used on any color coordinate system to segment and classify objects on the basis of color.

Users can add the package to a Raster Ops Color Board 364 Nubus card to grab images from NTSC composite or super VHS sources such as cameras or video recorders.

The software requires a Macintosh II computer with at least 4 Mbytes of RAM, a hard disk, and the color board. IP Lab Spectrum-364 costs \$1,049.

**Reader Service 40**

## System converts paper documents to image data

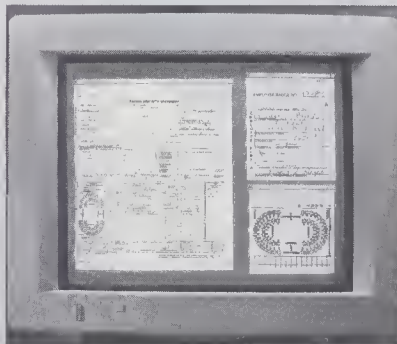
The DEC Image Express document management system captures images from applications running on Unix, OS/2, MS-DOS, and Macintosh platforms.

The DEC Image 1200 X windowing terminal lets a host application transport compressed images of patient documents for increased storage and record management. Image-acceleration hardware works directly on compressed images to support scaling, clipping, zooming, panning, and rotating.

Input from CCITT III fax machines and scanners converts paper documents to image data for indexing, display, and printing.

The DEC Image Express system starts at \$250,000. The 1200 will become a standard component by late April. With a 15-inch monitor, it costs \$3,395; the 19-inch size is \$4,095.

**Reader Service 41**



**The DEC Image 1200 Terminal monitor features a 100-dpi resolution and a 72-Hz refresh rate.**

## Window manager runs on X terminals

Network Computing Devices' window manager appears and behaves like Open Systems Foundation Motif and runs locally on X terminals.

NCDwm uses 100 Kbytes of memory and supports eight local terminal emulations simultaneously. Users can communicate with non-X applications via Digital Equipment Corp. local area transport, transmission-control/Internet protocol Telnet, or the X terminal local serial port.

NCD terminals run both the server and client functions of window manager and terminal emulation, which normally reside on the host.

A remote reset function allows units to be centrally restarted and downloaded with new software/configuration parameters.

The software is free to current users with the NCD software support program and \$500 per site for others.

**Reader Service 42**

## Add-on option for IBM mainframes

Network Sharefile from STSC Inc. provides transparent and concurrent access to multiple APL files and work spaces running on virtual machine- and MVS-based systems and on one or more CPUs.

The option enables a large server to partition into smaller ones while still appearing as a single server. This reputedly reduces the impact of hardware failures and increases the backup speed.

**Reader Service 43**

## SDLC transport available on Cisco routers

Cisco Systems' internetwork router/bridges now support IBM synchronous data link control (SDLC) protocol, which facilitates communication among remote IBM Systems Network Architecture devices.

SDLC software enables IBM mainframe front-end processors and cluster

# Local area networks

controllers to communicate through Cisco routers, allowing their data to share a pipeline with other protocols.

The software encapsulates SDLC traffic in Internet protocol packets and uses a Cisco interior gateway protocol to route them over IP networks, which include serial lines, FDDIs, Ethernets, and token rings.

The upgrade is free to current users and \$500 for others.

**Reader Service 44**

## Coaxial bridge links PCs to LANs

Harris Adacom Corp. announced a coaxial bridge to hook up PCs to Novell/Netware local area networks. Coax Net provides LAN functionality and services to coax-attached PCs or PS/2s without the addition of a LAN board.

When the PC is attached by the bridge to an Ethernet or token-ring LAN running Novell/Netware, all LAN services and capabilities are enabled on Coax Net or across the network transparently, according to the company.

Coax Net PCs can access file servers and printers on the network, use electronic mail, and share databases across the LAN. The PCs can configure to support multiple devices. Each port can support a file server, bridge, workstation, or 3270 gateway.

The product ranges from \$8,000 to \$10,000, depending on configuration.

**Reader Service 45**

## Micro Technology enhances network management

Lance/NMS Release 2.1 incorporates fault isolation and network simulation features in its SNMP-based system.

The management system enhances network interoperability by monitoring and managing multivendor, multisegment networks.

A segment profiler allows the user to generate traffic profiles for any selected network segment. A station profiler examines the amount, rate, source, and destination of network traffic that is transmitted or received by a particular station.

The traffic generator tool evaluates the effect of different data loads on network performance.

The segment and station traffic profilers operate on Unix, Ultrix, and VMS-based systems. The traffic generator runs on the Sun operating system platform.

Lance/NMS Release 2.1 costs \$18,500.

**Reader Service 46**

## LAT technology available for Hewlett-Packard

Control Data's Ascent Link Unix communications package integrates Unix HP 9000 computers into DEC local area transport networks. The terminal network off-loads most of the character processing from the host computer onto a terminal server, freeing the host for other operations.

An HP 9000 running this software provides both LAT host and server functions. Multiple sessions, reverse LAT, and a constantly updated directory of available services are featured.

Ascent Link shares a common Ethernet interface with other communication protocols, such as transmission-control/Internet protocol and Ascent DNI (DEC-net interface).

**Reader Service 47**

## Synernetics extends LANplex multiplexers

The LANplex 5004 four-slot system supports environments with distributed clusters of computing equipment where minimal expansion capability is required.

Like others in its series, the modular, intelligent multiplexer supports network concentration and bridging in a single architecture.

LANplex 5004 ships during the third quarter of 1991. Prices begin at \$24,250, depending on configuration.

**Reader Service 48**

## LAN Hawk expands compatibility

LAN Hawk has enhanced its 5750 network center to include both single- and

multimode FDDI compatibility. A single-mode fiber contains a smaller core and uses laser technology — rather than a light-emitting diode. Light can travel farther, allowing the FDDI ring to expand beyond its 200K boundary.

Users can buy a multimode 5750 and switch cables for single-mode FDDI applications. A fiber optic splitter enables cable switching and passive attachment to the FDDI ring.

Portable additions to the network analyzer line provide the same functions as the 5750.

**Reader Service 49**

## Bridge routers announced

The Network Systems 6800 modular bridge router for LAN and synchronous WAN networks features a 16-card, 800-Mbps chassis.

The 6400, a modular LAN/WAN (wide-area network) bridge router with a six-card, 400-Mbps chassis comes with various interfaces for FDDI rings, communication links at speeds of up to 44.7 Mbps, and multiple Ethernets.

In both these products, the protocol processor and interface processors contain private memory and share global memory. They work with any option that fits within the available bandwidth and back panel.

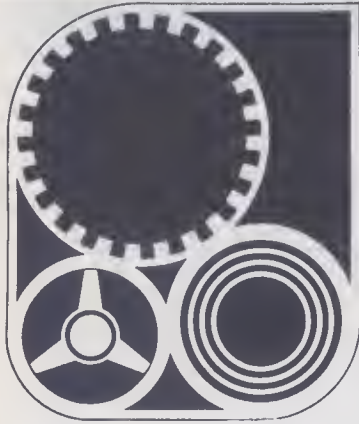
The 6600 single-board chassis with dual-access FDDI and LAN/WAN interfaces features up to four Ethernet ports, or two Ethernet and two synchronous ports. These ports support line speeds up to 2,048 Mbps. Options include additional Ethernet connections, a second communication link, and an FDDI interface.

For the 6000 series, network software includes security and administration, network management functions, a learning bridge with spanning tree, and routing protocols.

The 6800 ships now, while the 6400 ships in April and the 6600 in June.

Prices start at \$5,500 for the 6600, \$16,600 for the 6400, and \$46,000 for the 6800.

**6400: Reader Service 50**  
**6600: Reader Service 51**  
**6800: Reader Service 52**



# 13TH INTERNATIONAL CONFERENCE ON SOFTWARE ENGINEERING

## SYSTEM DESIGN: RESEARCH & PRACTICE

Stouffer Hotel ■ Austin, Texas ■ May 13-16, 1991

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**Keynote Address:** Craig Fields  
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Butler Lampson

### TUTORIALS - May 12-13, 1991

1. Formal Methods
2. Real-Time Systems Design
3. Visual Programming Environments
4. Modeling Measuring and Managing the Software Development Process: The M3 Lifeboat for Software Tarbits
5. Software Reliability Engineering
6. Software Technology Transition
7. CASE Tools for Requirements and Design
8. Usability Engineering
9. Software Engineering Support for Future Supercomputing Systems
10. Principles of System Engineering Management
11. Applying TQM to Software Systems
12. The SEI Framework for Software Process Improvement
13. Risk Management of Software Projects
14. State-of-the-Art in Environment Support for CM

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#### PARALLEL SESSIONS

A Methodology for Prototyping-in-the-Large  
Towards Cost-Effective Formal Specification  
Using Weaves for Software Construction and Analysis  
The International State of Practice  
Understanding Natural Programs Using Proper Decomposition  
Toward New Techniques to Assess the Software Implementation Process  
An Intelligent Tool for Re-engineering Software Modularity  
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Designing Software Applications for Use by Humans, not Machines  
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PRESTIGE: A CASE Workbench for the JSD Implementor  
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Parameter Value Computation by Least Square Method and Evaluation of Software Availability and Reliability at Service-Operation by the Hyper-Geometric Distribution Software Reliability Growth Model  
Integrating Prior Knowledge with a Software Reliability Growth Model (Experience Report)  
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Software Reuse in an Industrial Setting: A Case Study  
A Look Backward: Influential Papers from ICSE-2 and ICSE-3

#### PANEL SESSIONS

Is Software Reuse Delivering?  
Non-Technological Aspects of Software Engineering  
Ethical Considerations for Software Engineers  
Software Engineering Environment Integration  
A Look Forward: Panel on Software Engineering in the 1990's

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Laurie & John Werth  
Department of Computer Sciences  
University of Texas at Austin  
Austin, TX 78712  
Phone: 512/471-9535 or 512/471-9583  
FAX: 512/471-8885  
EMAIL: lwerth@cs.utexas.edu or jwerth@cs.utexas.edu

### ASSOCIATED WORKSHOPS-MAY 13, 1991

Workshop on Directions in Software Engineering Education

Contact: Laurie and John Werth  
(see above information)

Workshop on Software/Hardware CoDesign

Contact: David Franke  
Phone: 512/338-3641  
Email: franke@mcc.com

Martin Purvis  
Phone: 512/338-3605  
Email: pruvism@mcc.com

Workshop on Domain Modeling for Software Engineering

Contact: Neil Iscoe  
Phone: 512/477-1892  
Email: iscoe@austin.eds.com

Gerald B. Williams  
Phone: 312/507-6672  
Email: williams@andersen.com

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### ADDITIONAL INFORMATION CONTACT:

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Austin, TX 78720  
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FAX: 512/338-3899  
Email: basmith@mcc.com



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- ☐ 2. Real-time Systems Design
- ☐ 3. Visual Programming Environments
- ☐ 4. Modeling Measuring and Managing the Software Development Process: The M3 Lifeboat for Software Tar pits
- ☐ 5. Software Reliability Engineering
- ☐ 6. Software Technology Transition
- ☐ 7. CASE Tools for Requirements and Design
- ☐ 8. Usability Engineering
- ☐ 9. Software Engineering Support for Future Supercomputing Systems
- ☐ 10. Principles of System Engineering Management
- ☐ 11. Applying TQM to Software Systems
- ☐ 12. The SEI Framework for Software Process Improvement
- ☐ 13. Risk Management of Software Projects
- ☐ 14. State-of-the-Art in Environment Support for CM

## Tutorial Registration - Price is per Tutorial

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Written requests for refunds must be received in the IEEE Computer Society office no later than April 12, 1991. Refunds are subject to a \$50 processing fee. All no-show registrations will be billed in full. Students are required to show current picture ID cards at the time of registration. Registrations after April 19, 1991 will be accepted on-site only.

# IC Announcements

Company, Model, Function

Comments

R.S. No.

|                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |     |
|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| AMP<br>Right-angle<br>connectors                        | Provide a 0.125-in. card slot height with liquid crystal polymer plastic latches and 0.160- and 0.250-in. card slot heights with metal latches for single- or dual-sided SIMM JEDEC module boards. Connectors with 0.100-in. contact centerline spacing come with a 0.250-in. card slot height. Options include gold or tin plating, LCP housings, and polarized posts. Cost (1,000s): About \$2 to \$3.                                                                                              | 120 |
| Analog Devices<br>AD7244/242<br>Monolithic ICs          | The AD244 dual 14-bit DAC and the pin-compatible 12-bit 242 version work with signal conversion applications. Come in 24-pin DIP or 28-lead SOIC packaging. Consume 130 mW (typical) from $\pm 5V$ supplies. The 14-bit version settles to $\pm 0.5$ LSP in less than 4 $\mu s$ , while the 12-bit version settles in at 3 $\mu s$ . Cost (100s): \$14.00 (12-bit); \$17.95 (14-bit).                                                                                                                 | 121 |
| ATM<br>ATS-1200<br>Inspection system                    | Bench-top inspection and lead correction system for SOIC packages combines scanning and straightening into one operation. Resets coplanarity and body offset height and straightens leads to JEDEC and EIAJ standards. Component throughput exceeds 2,500 pph. Uses a single track-way and guide rail to minimize snagging and misalignment. No price given.                                                                                                                                          | 122 |
| Cirrus Logic<br>CL-SH351<br>Controller chip             | Designed for workstation and minicomputer applications, the chip contains hardware to build a SCSI-2 Winchester disk-drive controller subsystem. Features a 10-Mbyte/sec. synchronous transfer rate and a 32-MHz disk-transfer rate. Supports embedded servo designs and zone recording formats. Comes in 100-lead quad flatpacks. Cost (100s): \$20 (first-quarter 1991 sample prices).                                                                                                              | 123 |
| Cirrus Logic<br>CL-SH370<br>Controller chip             | Designed for small-footprint workstations and laptop/notebook computers, the chip contains hardware to build a SCSI Winchester disk-drive subsystem. Features a 5-Mbyte/sec. synchronous data rate and a 3-Mbyte/sec. asynchronous data rate for host bus transfers. Supports zone recording formats, split data field capability, and a 32-MHz nonreturn-to-zero data rate with data streaming. Comes in 100-lead quad flatpacks. Cost (100s): \$22.00 (first-quarter 1991 sample prices).           | 124 |
| Fujitsu<br>MB3780A<br>Battery backup IC                 | Works with SRAMs, ROMs, and logic IC devices by automatically switching to two alternate power sources during DC power loss or disturbance. Features a 1.0 mA standby current, 200 mA drive current, and 230 mV input-to-output voltage differential. Provides input loss voltage detection level of 4.2V $\pm$ 2.5 percent and on-chip secondary 2.8V rechargeable battery. Comes in 16- or 20-pin plastic DIPs and 16- or 20-pin plastic flatpacks. Cost (1,000s): \$1.15 (DIP); \$1.50 (flatpack). | 125 |
| Fujitsu<br>MB86021/22/23<br>DACs                        | Four-channel 8-bit converters contain internal data latches that support direct parallel-data interface with microprocessors and similar devices. The 021 and 022 operate at a 200 KSPS conversion rate, while the 023 operates at 500 KSPS. Devices contain external and internal reference voltage generators and operate on either a single 5V or dual $\pm 5V$ power supply. Come in 24-pin plastic DIP or plastic flatpacks. Cost (1,000s): \$3.77, MB86021/22; \$4.12, MB86023.                 | 126 |
| Hitachi<br>HD74BC series<br>Logic ICs                   | The 8-bit bus transceivers (245P and 645P/FP) offer on-chip pull-up resistors, a $-40^{\circ}C$ to $+85^{\circ}C$ temperature range, and thin, small-outline surface mount packaging. Feature typical 4.5-ns gate-propagation delay and a driving current of 64 mA at 10 MHz. Cost (100s): \$1.10, 245P (plastic DIP); \$1.25, 245FP (flatpack); \$1.55, 645 (plastic DIP); \$1.70, 645FP (flatpack).                                                                                                 | 127 |
| Intel<br>85C060-10<br>$\mu$ PLD                         | Microcomputer-programmable logic device runs at 10 ns and features a 100-MHz counter frequency. Internal speeds reach up to 100 MHz. The 16-macrocell CMOS device comes in 24-pin plastic DIPs and integrates multiple devices into one. Designed for laptop and portable computer applications. Cost (1,000s): \$19.44.                                                                                                                                                                              | 128 |
| Siemens<br>HYB511610-60/80<br>DRAM                      | The 16-bit DRAM includes more than 33 million transistors on a 142-sq. mm silicon chip and features a 16,777,216-bit capacity (equivalent to 1,000 typed pages). Comes in 16-Mbit $\times$ 1 and 4-Mbit $\times$ 4 configurations with 60- and 80-ns access speeds. Prototypes come in J-leaded prototype packages; sample 16-Mbit parts come in 24-pin zigzag-inline packages. No cost given.                                                                                                        | 129 |
| Texas Instruments<br>'ACT2235/36<br>Bidirectional FIFOs | Memory devices run at up to 50 MHz with access times as low as 25 ns. Feature high-output drive for direct bus interface. Includes '652 and '646-type control logic and support eight (2235) or five (2236) bus management functions. Feature asynchronous operation between read and write clocks, cascable width, and programmable almost full/almost empty flags. Come in PLCC packaging. Cost (1,000s): From \$22.32 (16.7-MHz) to \$51.12 (50-MHz).                                              | 130 |

# Microsystem Announcements

Company, Model, Function

Comments

R.S. No.

|                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |     |
|--------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Analogic<br>FG/ALU-8<br>Frame grabber                              | Intelligent frame grabber features arithmetic logic unit for real-time on-board processing, a frame buffer, a software library, and RGB outputs. Accommodates up to four inputs and includes an antialiasing filter, compatibility with video formats, and 8-bit resolution. Stores and processes 32 frames. IBM PC AT-compatible. Cost: From \$3,395 (quantity discounts available).                                                                                                   | 135 |
| Avalon Computer<br>Systems<br>Vaccelerator AP/30<br>RISC processor | Coprocessor for VAX and MicroVAX systems runs VMS applications without modification. The 33-MHz RISC processor benchmarks at up to 36 VAX MIPS. Scalar processor features 4-Mbyte memory and works with Q-bus or Unibus expansion slots. Up to 10 boards can run on a VAX for the same or separate applications. Comes with Fortran compiler. Cost: \$17,390.                                                                                                                           | 136 |
| Computer System<br>Architects<br>Transputer Education Kit          | Resulting from an agreement among CSA, Inmos, and Logical Systems, the kit includes a PC add-in board with a 20-MHz 32-bit transputer, two compilers (Occam and C), an assembler, and 1,500 pages of documentation. Multiple transputers form large processor networks for parallel processing. Options include up to 4 Mbytes of local DRAM, an upgraded transputer (20, 25, or 30 MHz), and upgraded software. Cost: \$236 (introductory price); \$150, add-on processor boards.      | 137 |
| Hewlett-Packard<br>HP 64700 series<br>Emulation/analysis tools     | Tools for National Semiconductor's 32-bit imaging microprocessors work with IBM PCs and HP 9000 Series 300 and 400 workstations. Emulators include a bus analyzer to trace microprocessor code flow. Dual analyzer buses allow traces to be set up and reviewed without breaking processor execution. Emulators provide software prestore function, symbolic debugging, and code-coverage analysis. Cost: From \$23,000 to \$28,000, depending on configuration.                        | 138 |
| Image and Signal<br>Processing<br>ISPx<br>Array processing boards  | Processing boards comes with one to four processors and from 4 to 16 Mbytes of memory. One board features design for medical imaging and data compression applications with real-time data handling requirements and can function as a master or a slave. Processors interlink and share a bus. Cost: \$3,995, ISP133; \$9,995, ISP433; others by quote.                                                                                                                                | 139 |
| Literal Corp.<br>ISI 525GB+<br>WORM disk drive                     | This 5.25-in. drive features an embedded SCSI-2 interface and transparent driver software that enables the system to simulate a hard drive. Connects with PC-compatible ISA or MCA systems and DEC Q-bus or Unibus systems. Cost: \$4,399 (with internal-mount drive); \$4,399 (external-mount drive); \$7,399 (with optical disk tower).                                                                                                                                               | 140 |
| Keithley Metrabyte<br>Das-temp<br>Measurement board                | The 32-channel, 12-bit temperature measurement board can measure 200 samples per second, and works with IBM PC XT/ATs. Operates in the -25°C to 105°C temperature range with a 0.1° minimum temperature resolution. Features manual or automatic calibration modes. Immune to most noise. Cost: \$399.                                                                                                                                                                                  | 141 |
| Landmark Research<br>Upgraded Kickstart 2<br>Test card             | Diagnostic card for IBM PC XT/AT and other ISA systems features preboot system diagnostics and password protection in EPROM and software-configurable I/O. Add-in card features eight bits and an AT-compatible basic I/O system for motherboards without power-on self-test codes. Cost: \$599.                                                                                                                                                                                        | 142 |
| Mercury Computer<br>Systems<br>MC860VB<br>Attached processor       | Attached processor based on the 40-MHz i860 features up to 40 MIPS/80 Mflops on a VMEcard for Sun-3, Sun-4, Silicon Graphics workstations, and real-time workstations running Vx Works. Transfers data over the VMEbus at 70 Mbyte/sec. Board interface provides a secondary bus to connect CPU boards, frame grabbers, and graphics boards, and features a peak transfer rate of 35 Mbytes/sec. Memory comes on daughterboard in 2-, 4-, 8-, or 16-Mbyte modules. Cost: From \$11,900. | 143 |
| Perceptive Solutions<br>Hyperstore 1600<br>Caching disk controller | Features a Z280 16-bit microprocessor for file servers, workstations, or PCs. Transfers data at up to 4 Mbytes/sec. and provides up to 50.4 Gbytes of mass storage and up to 20 Mbytes of RAM cache. Multitasking operating system concurrently manages and executes several tasks and accesses multiple daughtercards. Supports major operating systems. Cost: \$900 (with/without drivers); from \$275 (daughtercards).                                                               | 144 |
| Velox Systems<br>Icejet 486<br>486 motherboard                     | Small-footprint motherboard benchmarks at 35.6 MIPS on Dhrystone 1.1, 22.4 MIPS on Power Meter 1.5, and 225 MIPS(extrapolated) on Landmark 1.14. The 8.5 x 13-in. board runs at 50 MHz and has seven IBM PC AT-compatible slots that run at 8 or 16 MHz. Supports up to 16-Mbytes of 70-ns interleaved page-mode memory and the Weitek 4167 coprocessor. Cost: \$3,400 (CPU and 1 Mbyte RAM).                                                                                           | 145 |

# International Conference Cognitive science: Tools for the Development of Organizations April 29 to May 2, 1991 Montréal



Organized by:  
GIRICO  
Université du Québec à Montréal

Sponsored by:  
ACI Association canadienne d'informatique  
AFCET Association française pour le  
cybernétique économique et technique  
BCS The British Computer Society  
CEFRIO Centre francophone de recherche en  
informatique des organisations  
CRIM Centre de recherche informatique de Montréal  
FIO Fédération de l'informatique du Québec  
INRIA Institut national de recherche en  
informatique et en automatique

In cooperation with:  
ACM Association for Computing Machinery  
SIGART, SIGOIS  
CSCSI Canadian Society for Computational  
Studies of Intelligence  
IEEE-CS IEEE Computer Society

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(Université du Québec à Montréal, Canada)

Program Co-Chairpersons:  
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## Conference Objective

The objective of this conference is to provide researchers and representatives from industry and government with an opportunity to:

- Present and discuss their research results
  - Review applications of artificial intelligence and expert systems in organizations
  - Discuss of future directions for research and development
- Ico'91 will include tutorials, and a three day scientific conference.

## Topics of Interest

The conference will primarily focus on the following areas:

- Impact of AI and CS in organizations and in industry
- Natural language processing
- Knowledge-based tools for management and decision support
- Knowledge representation and acquisition
- Intelligent tutoring systems for training
- Computer-aided manufacturing and industrial robotics
- Evaluation of working systems.

A simultaneous translation service will be provided for the participants.

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**Jean-Pierre Desclés**

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**Brian Gaines**

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**Jean-Guy Meunier**

Université du Québec à Montréal, Canada

**Beverly S. Woolf**

University of Massachusetts, USA

## Accommodation

Rooms are reserved at the Hôtel des Gouverneurs, near the conference location. These rooms will only be held until March 28th, after which time availability cannot be guaranteed. Participants are asked to reserve as soon as possible and mention ICO'91.

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| Members of sponsoring or cooperating organizations | 290(Can.\$)      | 345(Can.\$) |
| Non-members                                        | 325              | 390         |
| Students                                           | 80               | 80          |
| Banquet (May 1st)                                  | 25               | 25          |
| Proceedings (Suppl. Copy)                          | 35               | 35          |
| Tutorials (each 1/2 day)                           | 110              | 130         |

Conference fees cover admission for conference sessions, simultaneous translation, lunches (except for students), coffee-breaks, and a copy of the proceedings. Tutorial fees include admission to tutorial, documentation available and coffee-breaks. Official taxes are included.

## For Further Information

Please contact:

Martine Fuentes

Fax: 1- (514) 987-8477

E-mail: ICO91 @ INFO.UQAM.CA

Phone: 1- (514) 987-3239

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# CONFERENCES

## Formal establishment of computer-based systems engineering field urged

Jonah Z. Lavi, Ashok K. Agrawala, Raymond Buhr, Ken Jackson, Michael Jackson, and Bernard Lang\*

Computer-based systems engineering should be established as a new discipline in its own right. To achieve that end, the IEEE Computer Society should set up a task force to promote the field, create CBSE institutes, and develop a CBSE educational framework.

Those were the major recommendations of participants at the IEEE Computer-Based Systems Engineering Workshop held last May in Neve-Ilan, Israel. The Israel Section of the IEEE and the Israel Chapter of the IEEE Computer Society organized the international event, with Jonah Z. Lavi serving as workshop chair.

An IEEE Computer Society Task Force on Computer-Based Software Engineering has since been established (see p. 76 of the February 1991 issue of *Computer*). The task force will conduct its first meeting May 13 in Austin, Texas, during the 13th International Conference on Software Engineering. The task force session will be devoted to organizational issues, deciding on objectives, and forming subcommittees.

**Workshop agenda.** Defining the CBSE discipline and discussing its current and future practice and ways to establish and promote it were the principal components of the workshop agenda.

Modern computer-based systems are complex multisystems that consist of many connected individual subsystems, each one typically a multicomputer system as well. The subsystems in a multisystem can be either geographically distributed, as in information systems, or locally connected, as in an aircraft avionics system. Other typical examples of computer-based systems are medical systems, process control systems, communications systems, and weapon systems.

Engineering these complex computer-based systems requires interdisciplinary techniques, methods, and skills that encompass different aspects of the field.

Despite the rapidly increasing demand

for engineers experienced in this new discipline, their supply is limited. This is due to a lack of (1) institutions that educate such engineers, (2) groups in academia and industry devoted to the research and development of methods and tools necessary in analysis and engineering, and (3) relevant conferences and journals. In addition, the industry does not have enough experienced engineers who can train the needed computer-based systems engineers on the job. As a result, many of the systems are developed without consideration of overall issues. This causes excessive development costs, delayed schedules, unnecessary development cycles, and poor performance. Many of these systems are also unsafe and unreliable.

Active engineers and experts in this emerging discipline were trained either in computer science or electrical engineering departments. Neither department is training computer-based systems engineers capable of handling the holistic problems and issues that have to be addressed during CBS development.

Software engineering curricula attempts to cope with the problem but, unfortunately, software engineering is taught mainly in individual courses and has not emerged as an independent university curriculum. One reason is that software engineering handles only a limited part of the issues involved in CBSE. Therefore, it is hard to sell software engineering as a discipline, both in academia and in industry.

Many have realized lately that a need exists to develop this new discipline. Indeed, the "Call for Papers" for the 13th International Conference on Software Engineering May 13-16 states that "the engineering of software is becoming the engineering of computerized applications." Therefore, the theme of ICSE 13, sponsored by the IEEE Computer Society and the ACM, is "Systems Design: Research and Practice."

**Workshop objectives.** The program committee of Comp Euro 90, also held last May in Israel, recognized this problem as well and selected "Systems Engineering Aspects of Complex Computer-Based Systems" as the theme of that

event. The Comp Euro committee further realized that this new discipline is not well-defined, that its tools and methods are not well established, and that it should be actively promoted. Thus, the IEEE Israel Section and the IEEE Computer Society Israel Chapter organized the CBSE workshop.

The major workshop goals were to

(1) Define the CBSE discipline, its contents and problems, and discuss the state of the art and the reasons why CBSE is not widely recognized as an active field of teaching and practice; and

(2) Discuss the promotion of CBSE as an acknowledged engineering discipline in industry and academia.

A program committee was formed, and a call for papers and participation was issued. Twenty position papers were submitted, and 28 people from nine countries participated. Three plenary sessions were held the first day of the event, with discussions on CBSE definition, practice, establishment, and promotion. Each session featured a kickoff panel with two to three participants followed by a discussion. The sessions helped get the participants acquainted with the workshop issues and with each other.

After the plenary sessions, the participants were divided into three working groups, one devoted to defining CBSE, another studying CBSE practice, and the third discussing how to establish and promote the discipline. Each group made a presentation at the final plenary session the afternoon of the workshop's second day. Despite their independent deliberations, the groups reached a clear consensus: that CBSE should be acknowledged as a new engineering discipline and promoted energetically.

One discussion delved whether this discipline is in fact merely a grouping of application-specific disciplines, such as process control, systems engineering, avionic systems engineering, and others. Participants agreed that it is not simply a grouping but a legitimate discipline by virtue of its own qualifications.

**Definition.** Computer-based systems engineering is an interdisciplinary branch

\*Lavi is with Israel Aircraft Industries; Agrawala, with the University of Maryland; Buhr, with Carleton University; Ken Jackson, with SD-SCICON UK Ltd.; Michael Jackson is a consultant in Great Britain; and Lang, with Institut National de Recherche en Informatique et en Automatique.

of engineering that merges systems, software, electronics, management, and application-specific techniques. It is concerned with the decomposition of systems, the allocation of development responsibility for specific system components (to specialist developers or manufacturers), and the subsequent composition of these system components to produce a final system. Its approach is holistic, involving trade-offs between the various specialist disciplines and the technical coordination of development efforts across the complete project.

Defining the class of computer-based systems explicitly is difficult. It can be described by listing the typical attributes, enumerating some of the engineering technologies that are important, and describing some of the existing scientific foundations of these technologies. A primary attribute of CBSE is that every relevant CBS includes major software and digital computer components. The other attributes can be divided into structural and behavioral attributes, a number of which were identified. Since these systems have major software and hardware components, all technologies of software and hardware development and design are clearly important. However, some seem to stand out as particularly important for CBS engineering as a whole. Synthesis technologies are good examples.

Many of the scientific foundations of CBSE technologies are simply the foundations of software or electrical engineering, including such traditional subjects as circuit theory and graph theory. Others are more directly concerned with

systems engineering than with the understanding and design of complex assemblies and structures. Among these are systems theory and control theory. Although not all the necessary scientific foundations for the discipline are currently identified, the missing ones will emerge as the field develops.

**CBSE practice.** In this branch of engineering, both practice and methods rely too heavily on the ingenuity of the designer. The engineering technologies necessary for the analysis and design of complex CBSs seem to be lacking. Especially wanting are the interdisciplinary "gluing techniques" needed to analyze how a system's components work together as an integrated system.

Other problems involve the unrealistic expectations and methods used in the field. For example, according to a widely accepted myth, top-down development is possible even though it is known to be a fallacy in systems engineering.

Another myth that pervades the industry, especially in the software aspects of CBSE, is the concept of the perfect and complete CBS specification. Such perfection never exists; systems have to be designed for change.

Workshop participants cited the use of incorrect methods as another problem. This problem is illustrated in the number of document-driven CBS projects, in the specification of projects that keep the implementation out of the requirement documents, and on the emphasis on logical designs neglecting the physical constraints.

Development of modern CBSs will re-

quire new methods and methodologies supporting the engineering of these complex systems. Methodologies were defined at the workshop as collections of techniques, processes, and heuristics. A particular methodology consists of techniques used to capture information in a particular format — such as electronic and mechanical diagrams — processes that are applied to organize the derivation and capture of the information using one or more of the techniques, and heuristics that show engineers how to proceed in specific circumstances.

Since existing techniques are not capable of capturing the complete information necessary for the requirement specification or design and analysis, supplementing the information captured by the more formal techniques with added descriptions in a natural language is necessary. It follows, then, that we should concentrate on developing specific new techniques that fill the gaps left in existing methodologies and, consequently, reduce the use of natural languages.

CBS development must involve rapid iteration early in the life cycle to arrive at a system architecture embodying the required constraints, functionality, and testability that can form the basis for estimation and planning with an acceptable level of risk. Thus, development might be envisioned as a multipass process driven by the need to reduce risk.

Figure 1 illustrates the future development process, which begins with an initial concept assumed to be fuzzy. Next comes an iterative derivation process initially concerned with gathering/creating information and then capturing the information in a form suitable for communication within the team responsible for the derivation. The same process is applied to creating the requirement and the design. This way, many ideas are rejected, and the embryo design is modified until the result is acceptable to the developers and the customers.

Figure 1 also shows a branch labeled trial implementation. This option exists because, for some systems, the only way to reduce risk to an acceptable level is to partially implement the system.

**Establishment and promotion.** The existence of any technical field or discipline depends entirely on its promoters and practitioners. Though the workshop activities clearly reveal an existing community consciously dealing with CBSE, members of the field must further assert its role, actions, and concerns. In particular, they must reinforce their ties and attract concerned professionals using conventional means, such as specialized forums (journals, conferences, and work-

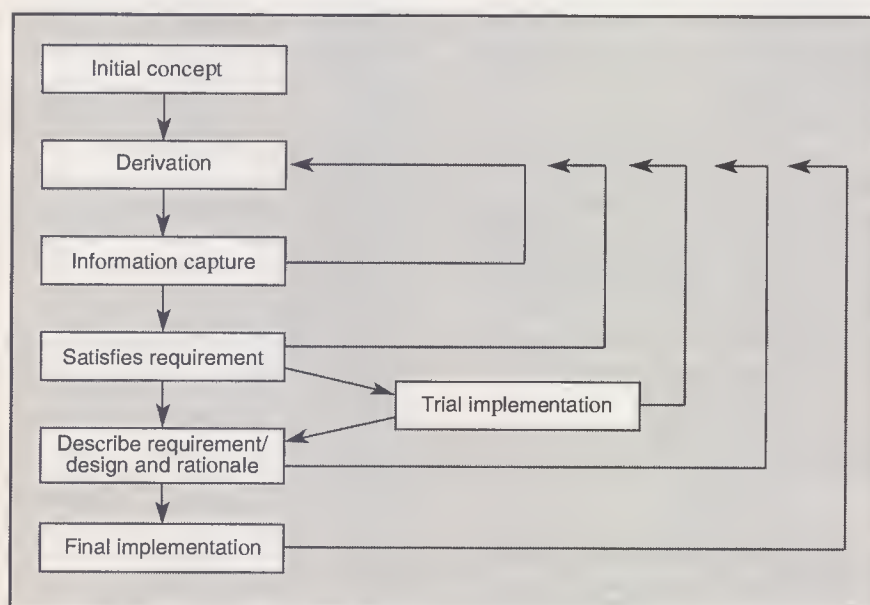


**Figure 1.** The future computer-based systems engineering development process and an additional branch labeled trial implementation.

shops) and recognized professional organizations.

Practicing CBS professionals learned their skills on the job, much as computer professionals did a quarter of a century ago. But this approach is expensive and cannot supply industry enough adequately educated professionals for the growing number of complex computer-based systems. Hence, an educational structure has to be developed to produce more CBS engineers, both by attracting people to this field and by making adequate curricula available.

The last requirement is for recognition by other communities. This will reinforce the internal identity of the CBSE community itself and make it better able to reach its goals.

Establishing an external identity requires lobbying and public relations to make CBSE better known. A careful analysis of CBSE's relationship to other fields of engineering and computer science will determine where they intersect and where they differ.

Clearly, CBSE can be promoted on many fronts. The first and most important recommendation of the workshop, to form a task force within the IEEE Computer Society to establish the identity of the field according to the suggestions made above, has been enacted. Other ways to promote CBSE include organizing additional workshops and conferences and advocating the need to establish research institutes with the necessary educational programs.

Creating one or more CBSE institutes to be the flagships of the field and, thus, giving CBSE visibility would be a major step toward achieving these objectives. More concretely, these institutes should research CBSE and CBSE-related fields. This research should include experimen-

tal work on large-scale CBSs. Systems that better exhibit real problems are often too large to be developed within an academic environment.

Another objective is education in cooperation with universities and industry. This activity should stress advanced teaching, especially with regard to experienced professionals. This would also include creation of new curricula and analysis of the effectiveness of existing curricula relative to the state of the art and present industrial needs.

In addition to research and educational objectives, another goal is technology transfer to industry, particularly through training of professionals on institute projects or simply by demonstrating those projects.

To be successful, such institutes must have the necessary equipment, human resources, and expertise. Considering the cost and complexity of the systems studied, large national or international institutions sponsored by government, industry, and academia will be required.

The institutes will strive to develop competence in all technical areas of concern to CBSE.

**Education issue.** CBSE education raises problems that require an original approach. The basic scientific knowledge required covers many scientific domains, which a single individual cannot grasp in depth. Hence, a proper balance has to be found in curricula to provide adequate knowledge in each. In some cases, finding unifying concepts might reduce the learning load. This should certainly be an object for CBSE research.

Much of the difficulty of CBSE is due to the size and complexity of the systems considered. Thus, an academic environment would need cooperation from in-

dustry or the proposed CBSE institutes, either through participation in a real CBSE project or through teaching professionals involved in such projects.

Those who teach the development and management of complete systems should have some professional experience and sufficient command of the supporting disciplines.

The workshop participants agreed that academic teaching of CBSE students should clearly distinguish between undergraduate and graduate education. While undergraduate education must concentrate on the supporting disciplines, it can also serve to sensitize students to the specific problems and complexities of CBSE.

However, in-depth CBSE training should be reserved for graduate-level education, addressing mature students who have some basic professional experience as support and motivation for their study.

Copies of the complete workshop report and the announcement for participation in the first meeting of the task force are available by contacting Ashok K. Agrawala, Department of Computer Science, University of Maryland, College Park, MD 20742, phone (301) 405-2665, e-mail [agrawala@cs.umd.edu](mailto:agrawala@cs.umd.edu); or Jonah Lavi, Dept. 9100, Israel Aircraft Industries, Ben Gurion International Airport, Israel, phone 972 (3) 935-3716. Please direct questions to Agrawala.

## Acknowledgments

The authors thank all the participants for their valuable contributions to the success of the workshop, especially H.U. Steusloff of Germany and A. Yehudai of Israel for service on the program committee.

## Tribe, Noam, Bayse to address Computers, Freedom, Privacy Conference

Laurence H. Tribe of the Harvard Law School, Eli M. Noam of Columbia University, and William A. Bayse of the FBI will be the key speakers at the First Conference on Computers, Freedom, and Privacy. The event is set March 25-28 at the San Francisco International Airport Marriott Hotel in Burlingame, Calif.

Subtitled "Pursuing Policies for the Information Age in the Bicentennial Year of the Bill of Rights," the conference is being sponsored by the Computer Professionals for Social Responsibility, with the IEEE, the IEEE Intellectual Property Committee, the IEEE-USA Committee on Communications and Information Policy, and the ACM among the cospon-

soring and cooperating organizations. Attendance will be limited to 600 persons due to the size of the facility.

Jim Warren of Autodesk Inc. and *MicroTimes* is serving as conference chair.

**Keynoters, program.** Tribe, a professor of constitutional law, will offer major policy proposals the morning of March 26 with a talk entitled "The Constitution in Cyberspace: Law and Liberty Beyond the Electronic Frontier."

Noam is director of the Center for Telecommunications and Information Studies at Columbia. He will talk on "Network Environments of the Future: Reconciling Free Speech and Freedom of

Association" on March 26.

Bayse, the FBI's assistant director of the Technical Services Division, will deliver his remarks, "NCIC-2000: Balancing Computer Security Capabilities with Privacy and Integrity," on March 27.

Half-day morning and afternoon tutorials are slated on March 25 entitled "How Computer Crime is Investigated," "Information Security," "How Computer Crackers Crack," "Computer Communications and the Global Matrix," "Low-Cost Networks and Computer Bulletin Board Systems," "Federal Legislation Impacting Computer Use," "Computer-Related Legislation Within States," and "Impacts on the US of Other Nations"

Privacy Initiatives." Tutorials registration is limited.

The single-track conference sessions set March 26-28 will include "The Constitution in the Information Age," "Electronic Speech, Press and Assembly," "Computer-Based Surveillance of Individuals," "Personal Information and Privacy," "Ethics and Education," "Trends in Computer Networks," "Law Enforcement Practices and Problems," "Law Enforcement and Civil Liberties," "Legislation and Regulation," "Access to Government Information," "International Perspectives and Impacts," and "Where Do We Go From Here?"

**Crucial issues.** According to Warren, the organizations sponsoring and cooperating in staging the conference are supporting it to enhance communication, understanding, and consensus about crucial issues.

"We are at a crossroads as individuals, organizations, and governments increasingly use and depend on computers and computer networks," Warren said, adding that within 10 years, most information will be utilized and exchanged electronically. "We are in the pivotal decade when computer facilities and policies worldwide will mature," he said. These facilities and policies can allow and encourage mass access to and use of great information processing and networking power, and can control potential abuse. For potent personal benefit, business improvement, and national well-being, information and its efficient access are becoming economically available to individuals, organizations, and governments. Such access can greatly enhance sound decisions based on timely access to essential knowledge," Warren said.

"Data on individuals and groups is being collected, computerized, and exchanged at an exponentially increasing rate within numerous agencies and organizations. This has great legitimate value, but has also prompted increasing concerns regarding issues of personal privacy," said Warren.

"To assure sound and equitable decisions, the public, the press, and a broad range of policy-makers must understand and openly discuss these issues, their interactions, and their implications for the future. To protect the fundamental freedoms and personal privacy that are the foundation of any free people, all parties must be informed, and all must share in shaping and enhancing the great potential of the Information Age," said Warren.

For more information, contact CFP Conference, 345 Swett Rd., Woodside, CA 94062, phone (415) 322-3778, fax (415) 851-2814, e-mail cfp@well.sf.ca.us.

# CALL FOR PAPERS

**J. of Internetworking Research and Experience** seeks original research papers for publication in 1991. Publisher: John Wiley and Sons. Submit paper or short technical note to Deborah L. Estrin, Computer Science Dept. mc0782, Univ. of Southern Calif., Los Angeles, CA 90089-0782, e-mail estrin@usc.edu.

**ANN 91, Second Int'l Conf. on Artificial Neural Networks:** Nov. 18-20, 1991, Bournemouth, UK. Sponsor: Institution of Electrical Engineers. Submit synopsis by **Mar. 28, 1991**, to IEEE Conf. Services, Savoy Place, London WC2R 0BL, UK, phone (071) 240-1871, fax (071) 240-7735.

**Int'l Workshop on Field Programmable Logic and Applications:** Sept. 4-6, 1991, Oxford, England. Submit 10 copies of 500-word abstract by **Mar. 28, 1991**, and full paper by **Aug. 15, 1991**, to Anna Morris, CPD Unit, Continuing Education Dept., Univ. of Oxford, Rewley House, 1 Wellington Square, Oxford, OX1 2JA, England, UK, fax 44 (865) 270-708, e-mail cpdmail@vax.ox.ac.uk.

**Fourth Midwest Unix and Open Systems Conf.:** Sept. 18-19, 1991, Detroit, Mich. Submit three copies of extended abstract by **Mar. 29, 1991**, and papers by **May 17, 1991**, to S.P. Rana, Computer Science Dept., Wayne State Univ., Detroit, MI 48202, phone (313) 577-2831, fax (313) 577-6868, Internet rana@cs.wayne.edu.

**Fifth Portuguese Conf. on Artificial Intelligence:** Oct. 1-3, 1991, Algarve, Portugal. Sponsor: Portuguese Assoc. for Artificial Intelligence. Submit four copies of paper by **Mar. 31, 1991**, to Pedro Barahona, Dep. de Informática, Univ. Nova de Lisboa, 2825 Monte da Caparica, Portugal, e-mail pb@fetunl.rccn.pt.

**IEEE Micro** seeks manuscripts for the December 1991 special issue on database machines. Submit six copies of manuscript by **Apr. 1, 1991**, to A. Abdelguerfi, Computer Science Dept., Univ. of New Orleans, Lakefront, LA 70148, phone (504) 286-7076, Bitnet macs@uno.

**Supercomputing 91:** Nov. 18-22, 1991, Albuquerque, N.M. Cosponsor: ACM. Submit paper by **Apr. 1, 1991**, to Ann Hayes, Supercomputing 91, MS B260, Los Alamos Nat'l Lab, Los Alamos, NM 87545, phone (505) 665-4506, fax (505) 665-4361, e-mail ahh@lanl.gov.

**IEEE Workshop on Visual Motion:** Oct. 6-9, 1991, Princeton, N.J. Submit four copies of complete paper by **Apr. 1, 1991**, to Peter Burt, David Sarnoff Research Center, 201 Washington Rd., Princeton, NJ 08540, e-mail burt@vision.sarnoff.com.

**Hot Chips III Symp.:** Aug. 26-27, 1991, Stanford, Calif. Sponsor: IEEE

Computer Society Tech. Committee on Microprocessors and Microcomputers. Submit extended abstract by **Apr. 1, 1991**, to Melissa Anderson, Silicon Graphics, 2011 N. Shoreline Blvd., PO Box 7311, Mountain View, CA 94039-7311, fax (415) 965-7651, e-mail mda@sgi.com.

**Conf. on Software Maintenance:** Oct. 14-17, 1991, Sorrento, Italy. Cosponsor: IEEE. Submit five copies of paper or experience report by **Apr. 1, 1991**, to Vaclav Rajlich, Computer Science Dept., Wayne State Univ., Detroit, MI 48202, phone (313) 577-5423, fax (313) 577-6868, e-mail vtr@cs.wayne.edu; or Malcolm Munro, Centre for Software Maintenance, Univ. of Durham, Durham, DH1 3LE, England, phone 44 (091) 374-2634, e-mail malcolm.munro@uk.ac.durham.

**Visualization 91:** Oct. 22-25, 1991, San Diego, Calif. Sponsor: IEEE Computer Soc. Technical Committee on Computer Graphics. Submit four copies of paper (and video) by **Apr. 1, 1991**, to Gregory M. Nielson, Computer Science Dept., Arizona State Univ., Rural Road and University, Tempe, AZ 85287-5406, phone (602) 965-2785.

**Int'l Workshop on Visual Languages:** Oct. 9-11, 1991, Kobe, Japan. Cosponsors: Hiroshima Univ., Univ. of Pittsburgh. Submit paper by **Apr. 1, 1991**, to Tadao Ichikawa, Eng. Faculty, Hiroshima Univ., Higashi-Hiroshima 724, Japan, phone 81 (824) 22-7029, e-mail ichikawa@jpnhuis.bitnet.

**Second Symp. on the Assessment of Software Development Tools:** Nov. 1991, New Orleans. Submit paper by **Apr. 1, 1991**, to Ez Nahouraii, IBM, 598/089, 6321 San Ignacio Ave., San Jose, CA 95119, phone (408) 281-5741, e-mail ez.nahouraii@compmail.com.

**PDCS 91, Fourth ISMM Int'l Conf. on Parallel and Distributed Computing and Systems:** Oct. 8-11, 1991, Washington, DC. Cosponsors: Int'l Soc. for Mini and Microcomputers, Tech. Committee on Computers. Submit three copies of manuscript for regular paper or 300-word abstract for short paper by **Apr. 1, 1991**, to R. Ammar, PDCS 91, U155, Computer Science and Eng. Dept., Univ. of Connecticut, Storrs, CT 06268, fax (203) 486-4817.

**16th Conf. on Local Computer Networks:** Oct. 14-17, 1991, Minneapolis, Minn. Cosponsor: IEEE Computer Soc. Tech. Committee on Computer Comm. Submit five copies of full paper by **Apr. 5, 1991**, to James F. Mollenauer, 16th LCN Conf., Artel Communications, 22 Kane Industrial Dr., Hudson, MA 01749, phone (508) 562-2100, fax (508) 562-6942.

**TA1 91, Third IEEE Computer Soc. Conf. on Tools for Artificial In-**

## Call for articles and referees for *Computer*

 *Computer* seeks articles for inclusion in upcoming special issues.

**Heterogeneous Distributed Database Systems** is the theme planned for the **December 1991** issue. See the August 1990 issue of *Computer* (p. 115) for complete information.

Eight copies of the complete manuscripts must be submitted by **April 1, 1991**. Notification of decisions is **July 1, 1991**, and the final version of each manuscript is due **September 1, 1991**.

Submissions and questions should be directed to Sudha Ram, Department of Management Information Systems, Eller School of Management, University of Arizona, Tucson, AZ 85721, phone (602) 621-2748, e-mail ram@mis.arizona.edu on Internet or ram@arizmis on Bitnet.

**Document Image Analysis Systems** is the theme planned for the **June 1992** issue. Manuscripts reporting survey, original research, design and development, and applications of document image analysis are sought immediately in the following areas:

- Business documents
- Engineering drawings and maps
- Textbooks and technical manuals
- Automated postal processing
- Fingerprint recognition
- Man-machine interface
- Music and other symbolic forms

A 300-word abstract of each manuscript must be submitted by **May 1, 1991**; 14 copies of the complete manuscript are due by **July 1, 1991**; notification of decisions is set **December 1, 1991**; and the deadline for submittal of the final version of each manuscript is **February 1, 1992**.

Submissions and questions should be directed to Rangachar Kasturi, Electrical and Computer Engineering Department, Pennsylvania State University, University Park, PA 16802, phone (814) 863-4254, e-mail kasturi@cmpe.psu.edu; or Lawrence O'Gorman, Room 3D-455, AT&T Bell Labs, Murray Hill, NJ 07974, phone (201) 582-7262, e-mail log@research.att.com.

**Wafer Scale Integration: Architectures and Algorithms** will be the theme of the **April 1992** issue. See p. 109 of the February 1991 issue for complete details.

A 300-word abstract of each manuscript is due not later than **May 1, 1991**. Twelve (12) copies of each complete manuscript are due by **June 15, 1991**. Notification of decisions is set **October 1, 1991**, and the deadline for submitting the final version of the manuscript is **December 1, 1991**.

Submissions and questions should be directed to W. Kent Fuchs, Center for Reliable and High-Performance Computing, Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, 1101 W. Springfield Ave., Urbana, IL 61801, phone (217) 333-9731, fax (217) 244-1764, e-mail fuchs@crhc.uiuc.edu. Questions can also be directed to Earl Swartzlander, Department of Electrical and Computer Engineering, ENS Building, Room 517, University of Texas at Austin, Austin, TX 78712, phone (512) 471-5923.

**Computer Architectures for Intelligent Systems** has been selected as the theme for the May 1992 special issue. Manuscripts are sought reporting architectures, languages, dependable operating systems, communication schemes for intelligent systems, and performance analysis.

Submit a 300-word abstract by **April 1, 1991**, and 12 copies of each manuscript by **June 1, 1991**, to Jayantha Herath, ECE Dept., Drexel Univ., Philadelphia, PA 19104, phone (215) 895-6758, fax (215) 895-1695, e-mail jheraz@ocs.drexel.edu.

*For submittal to Computer, manuscripts must not have been previously published or currently submitted for publication elsewhere. Each manuscript should be no more than 32 typewritten, double-spaced pages long, including all text, figures, and references. Each submittal should include a cover page that contains the title of the article, the full name(s) and affiliation(s) of the author(s), complete postal and electronic address(es) of all the authors as well as their telephone and fax number(s), a 300-word abstract, and a list of keywords identifying the central issues of the manuscript's contents. The final manuscript should be approximately 8,000 words in length and contain no more than 12 references.*

*If you are willing to review articles for any of these special issues, please send a note listing your research interests to Jon T. Butler, editor-in-chief of Computer, or to one of the guest editors listed for the particular issue. Butler may be reached at the Department of Electrical and Computer Engineering, Naval Postgraduate School, Code EC/Bu, Monterey, CA 92943-5004, phone (408) 646-3299 or (408) 646-3041, fax (408) 646-2760, Internet butler@ece.nps.navy.mil.*

**telligence:** Nov. 10-13, 1991, San Jose, Calif. Submit five copies of abstract and full paper by **Apr. 10, 1991**, to Benjamin Wah, Coordinated Science Lab, MC 228, Univ. of Illinois, 1101 W. Springfield Ave., Urbana, IL 61801-3082, phone (217) 333-3516, fax (217) 244-1764, e-mail wah@aquinas@uxc.cso.uiuc.edu.

 **ICCAD 91, IEEE Int'l Conf. on Computer-Aided Design:** Nov. 10-14, 1991, Santa Clara, Calif. Cosponsor: IEEE Circuits and Systems Soc. Submit 12 copies of one-paragraph abstract and 12 copies of complete paper by **Apr. 12,**

**1991**, to ICCAD 91, MP Associates, 7490 Clubhouse Rd., Suite 102, Boulder, CO 80301, phone (303) 530-4562.

**Hypertext 91:** Dec. 15-18, 1991, San Antonio, Texas. Sponsor: ACM. Submit paper by **Apr. 12, 1991**, to Janet H. Walker, Hypertext 91, DEC, Cambridge Research Lab, 1 Kendall Square, Bldg. 700, Cambridge, MA 02139, phone (617) 621-6618, fax (617) 621-6650, e-mail jwalker@cri.dec.com.

 **Crypto 91:** Aug. 11-15, 1991, Santa Barbara, Calif. Cosponsors: Int'l Assoc. for Cryptologic Research et al. Submit 15 cop-

ies of detailed abstract by **Apr. 15, 1991**, and paper by **July 8, 1991**, to Joan Feigenbaum, Crypto 91, AT&T Bell Labs, Rm. 2C473, 6000 Mountain Ave., Murray Hill, NJ 07974, phone (908) 582-6910, Internet: jf@research.att.com.

 **First Int'l Conf. on Artificial Intelligence Applications on Wall St.:** Oct. 9-11, 1991, New York City. Sponsor: Polytechnic Univ., Brooklyn. Submit three copies of extended abstract by **Apr. 15, 1991**, and final paper by **July 1, 1991**, to Roy S. Freedman, Polytechnic Univ., 333 Jay St., Brooklyn NY 11201, phone (718) 260-3307, fax (718) 260-3136.

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**Advance Program**  
**18th Intl. Symposium on**  
**Computer Architecture**

May 27-30, 1991  Toronto, Canada



Sponsored by  
Association for Computing Machinery   
Institute of Electrical and Electronics Engineers  
IEEE Computer Society

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**CONFERENCE SITE:**

All technical sessions and registration will be held at the Royal York Hotel in the heart of downtown Toronto. The hotel is within walking distance to many attractions, including the CN Tower, the world's tallest free-standing structure, and SkyDome with its retractable roof. On Tuesday evening we will go to the Ontario Science Centre for dinner and an evening where you will be free to enjoy the exhibits.

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**Monday, May 27      Tutorials**

**Theme I: "Exploiting Concurrency"**

This theme discusses techniques and issues involved in exploiting concurrency. The morning tutorial concentrates on hardware issues and the afternoon concentrates on compilation issues.

*Morning Tutorial (#1): "Approaches to Concurrency (VLIW, HPS, Pipelining and RISC)" Speaker: Y.L. PATT*

Architectural choices available with respect to various approaches to exploiting concurrency. Compile time vs run-time alternatives, instruction sets, issuing alternatives.

*Afternoon Tutorial (#2): "Compilation Support for Superscalar Processors" Speaker: W. HWU*

Code Optimization Techniques and Scope, Code Scheduling methods, Critical Architectural Issues, and a discussion of Support of Numeric Applications vs. Non-numerical Applications.

**Theme II: "MIMD Synchronization and Coherency"**

This theme formulates the domain of synchronization and coherence concepts in an integrated and general manner, solving several outstanding problems in this domain. The treatment will apply to shared-memory and message-passing architectures, multiprocessor or distributed.

*Morning Tutorial (#3): "Synchronization and Access Order" Speaker: P. BITAR*

Identify fundamental synchronization options, and cover methods for handling out-of-order memory access.

*Afternoon Tutorial (#4): "Combining Trees and Coherence" Speaker: P. BITAR*

Analyze the motivation, structure, and management of combining trees, and discuss fundamental coherence options.

**Theme III: "RISC Systems: Architecture and Implementation"**

This theme presents the basic principles of RISC systems architecture and their design issues. CMOS and GaAs examples are discussed. The theme is intended for practicing engineers, computer scientists and graduate students.

*Morning Tutorial (#5): Speaker: V.M. MILUTINOVIC*  
RISC Principles, advantages and disadvantages, VLSI and compiler issues, examples (including RISC I,II, and Stanford MIPS).

*Afternoon Tutorial (#6): Speaker: D. TABAK*

Architecture, Structure, Performance Comparisons, applications in workstations, multiprocessors and real-time systems, examples (including 80860, IBM RISC System/6000, 88000, SPARC and MIPS).

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**Tuesday, May 28      KEYNOTE ADDRESS:**

Dr. Peter W. Smith, Bellcore

*"Optics in Computing - A Glimpse of the Future"*

**Session 1A: Application-Specific Processors**

*"The SNAP-1 Parallel AI Prototype", D. Moldovan*

*"GT-EP: A Novel High-Performance Real-Time Architecture", W.S. Tan, S. Russ, C.O. Alford*

*"IXM2: A Parallel Associative Processor", T. Higuchi, K. Handa, T. Furuya, N. Takahashi, A. Kokubu*

**Session 1B: Data Prefetching and Branch Prediction**

*"An Optimized Branch Penalty Reduction Strategy", D. Kaeli and P. Emma*

*"An Architecture for Software-Controlled Data Prefetching", A.C. Klaiber, H.M. Levy*

*"Data Prefetching in Multiprocessor Vector Cache Memories", J.W.C. Fu, J.H. Patel*

**Session 2A: Memory Architecture**

*"Reducing Memory Contention in Shared Memory Multiprocessors", D.T. Harper, III*

*"Pseudo-Randomly Interleaved Memory", B.R. Rau*

*"Evaluation of Memory System Extensions", K. Li, K. Peterson*

**Session 2B: Interconnection Networks**

*"High Performance Interprocessor Communication Through Optical Wavelength Division Multiple Access Channels", P.W. Dowd*

*"Race-free Interconnection Networks and Multiprocessor Consistency", A. Landin, E. Hagersten*

*"Deadlock-Free Multicast Wormhole Routing in Multicomputer Networks", X. Lin, L.M. Ni*

**Session 3: PANEL 1: (to be arranged)**

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**Wednesday, May 29**

**Session 4A: Caching**

*"Dynamic Base Register Caching: A Technique for Reducing Address Bus Width", M.K. Farrrens, A. Park*

*"Implementing a Cache for a High-Performance GaAs Microprocessor", O.A. Olukotun, T.N. Mudge, R.B. Brown*

**Session 4B: Processor Architecture**

*"Classification and Performance Evaluation of Instruction Buffering Techniques", L. Kurian, P.T. Hulina, L.D. Coraor, D.N. Mannai*

*"OHMEGA: A VLSI Processor Architecture for Numerical Applications", M. Nakajima, H. Nakano, Y. Nakakura, T. Yoshida, Y. Goi, et al.*

**Session 5A: Performance Evaluation of Real Machines**

*"An Empirical Study of the CRAY Y-MP Processor using the PERFECT Club Benchmarks", S. Vajapeyam, G.S. Shoi, W.-C. Hsu*

*"Instruction Level Profiling and Evaluation of the IBM RS/6000", C. Stephens, B. Cogswell, J. Heinlein, G. Palmer, J.P. Shen*

*"Performance Tuning and Prediction on a Multiprocessor", R.T. Dimpsey, R.K. Iyer*

**Session 5B: Multicomputer Communications**

*"Performance Evaluation of a Communication System for Transputer-Networks Based on Monitored Event Traces", C.-W. Oehlrich, A. Quick*

*"Chaos Router: Architecture and Performance", L. Snyder, S. Konstantinidou*

*"Scheduling Pipelined Communication in Distributed Memory Multiprocessors for Real-Time Applications", S.B. Shukla, D.P. Agrawal*

**Session 6A: Shared-Memory Multiprocessors**

*"Debugging Programs on Weak Memory Systems", M. Hill, B. Miller, R. Netzer, S.V. Adve*

*"On the Validity of Trace-Driven Simulation for Multiprocessors", E.J. Koldinger, S.J. Eggers, H.M. Levy*

*"Comparative Evaluation of Latency Reducing and Tolerating Techniques", A. Gupta, J. Hennessy, K. Gharachorloo, T. Mowry, W.-D. Weber*

### Session 6B: Instruction-Level Parallelism

"IMPACT: An Architectural Framework for Multiple-Instruction-Issue Processors", P.P. Chang, S.A. Mahike, W.Y. Chen, N.J. Warter, W-m. W. Hwu  
"Single Instruction Stream Parallelism is Greater Than Two", M. Butler, T-Y. Yeh, Y. Patt  
"Exploiting Fine-Grained Parallelism Through Combined Hardware and Software Techniques", S. Melvin, Y. Patt

### Session 7: PANEL 2: "To Cache or Not To Cache"

Thursday, May 30

#### Session 8A: "Cache Coherence"

"Modeling the Performance of Limited Pointers Directories for Cache Coherence", R. Simoni, M. Horowitz  
"Comparison of Hardware and Software Cache Coherence Schemes", S.V. Adve, V.S. Adve, M.D. Hill, M.K. Vernon

#### Session 8B: Register Sets

"Flexible Register Management for Sequential Programs", D.J. Quammen, D.R. Miller  
"The Effect on RISC Performance of Register Set Size and Structure Versus Code Generation Strategy", D.G. Bradlee, S.J. Eggers, R.R. Henry

#### Session 9A: Multithreading and Pipelining

"Multithreading: A Revisionist View of Dataflow Architectures", G.M. Papadopoulos, K.R. Traub  
"Multi-threaded Vectorization", T-C. Chiueh  
"Strategies for Achieving Improved Processor Throughput", M.K. Farrens, A.R. Pleszkun

#### Session 9B: Miscellany

"Adaptive Storage Management for Very Large Virtual/Real Storage Systems", T. Kagimasa, K. Takahashi, T. Mori, S. Yoshizumi  
"Virtualizing the VAX Architecture", J.S. Hall, P.T. Robinson  
"Modeling and Measurement of the Impact of Input/Output on System Performance", J. Akella, D.P. Siewiorek

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Conference registration includes one copy of the proceedings, Wednesday luncheon and reception, breaks, and the Ontario Science Centre. Tutorial registration includes one copy of notes and breaks. Please be sure to indicate the tutorial numbers on the registration form.

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# CALENDAR

## March 1991

**Φ Symp. on Experiences with Distributed and Multiprocessor Systems, Mar. 21-22, Atlanta.** Sponsor: Usenix Assoc. Contact George Leach, AT&T Paradyne, MS LG-129, PO Box 2826, Largo, FL 34649-2826, phone (813) 530-2376, e-mail reggie@pdn.paradyne.com.

**NIST Lecture Series on High-Integrity Systems, Mar. 22, Gaithersburg, Md.** Sponsor: National Inst. of Standards and Technology. Speaker: Victor Basili, Univ. of Maryland. Contact Dolores Wallace, NIST, Gaithersburg, MD 20899, phone (301) 975-3340.

**Fifth SIAM Conf. on Parallel Processing and Scientific Computing, Mar. 25-27, Houston.** Contact Soc. for Industrial and Applied Math. Conf. Coordinator, Dept. CC0590, 3600 University City Science Center, Philadelphia, PA 19104-2688, phone (215) 382-9800, fax (215) 386-7999, e-mail siamconfs@wharton.upenn.edu.

**Advanced Research in VLSI Conf., Mar. 25-27, Santa Cruz, Calif.** Sponsors: Univ. of California at Santa Cruz, Univ. of California at Berkeley. Contact Kevin Karplus, Computer Eng., Univ. of California at Santa Cruz, Santa Cruz, CA 95064, Internet karplus@ce.ucsc.edu.

**Auto Carto 10, 10th Int'l Symp. on Automated Cartography, Mar. 25-28, Baltimore.** Cosponsors: Am. Cartographic Assoc. et al. Contact ACSM/ASPRS/Auto Carto 10, 5410 Grovesnor Lane, Bethesda, MD 20814.

**First Conf. on Computer, Freedom, and Privacy, Mar. 25-28, Burlingame, Calif.** Cosponsors: Computer Professionals for Social Responsibility et al. Contact CFP Conf., 345 Swett Rd., Woodside, CA 94062, phone (415) 322-3778 or (415) 851-7075, fax (415) 851-2814, e-mail cfp@well.sf.ca.us.

**Control 91, Mar. 25-28, Edinburgh, Scotland.** Sponsor: Institution of Electrical Engineers. Contact IEE, PO Box 193, London WC2R 0QT, UK, phone (071) 240-1871, fax (071) 497-3633.

**Southcon 91, Mar. 26-28, Atlanta.** Sponsors: IEEE, Electronic Representatives Assoc. Contact Southcon, 8110 Airport Blvd., Los Angeles, CA 90045, phone (800) 877-2668, fax (213) 641-5117.

**CEEDA 91, Int'l Conf. on Concurrent Eng. and Electronic Design Automation, Mar. 26-28, Bournemouth, Dorset, UK.** Sponsors: Institution of Electrical Engineers et al. Contact Sa'ad Medhat, Bournemouth Polytechnic, Poole House, Talbot Campus, Fern Barrow,

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The above-mentioned information should arrive at **Computer** at least five weeks before the month of publication (i.e., for the May 1991 issue, send information for receipt by March 20, 1991) to Chuck Governale, Calendar Dept., **Computer**, PO Box 3014, Los Alamitos, CA 90720-1264, fax (714) 821-4010, e-mail c.governale@compmail.com.

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**DB/Expo 91, Nat'l Database Exposition and Conf., Mar. 26-28, San Francisco.** Contact NDN Enterprises, 289 S. San Antonio Rd., Suite 204, Los Altos, CA 94022, phone (415) 941-8440 or (800) 2DB-EXPO, fax (415) 941-2066.

**10th IEEE Int'l Phoenix Conf. on Computers and Comm., Mar. 27-30, Scottsdale, Ariz.** Sponsors: IEEE, IEEE Comm. Soc. Contact Mary Murphy-Hoye, phone (602) 554-5257, e-mail mhoye@fa.intel.com; or Oris Friesen, Bull HN, PO Box 8000, MS A93, Phoenix, AZ 85066, phone (602) 862-5200, e-mail friesen@system-m.phx.bull.com.

**Φ 1991 Multichip Module Workshop, Mar. 28-29, Santa Cruz, Calif.** Cosponsor: Nat'l Science Foundation. Contact Wayne Wei-Ming Dai, 313A Applied Sciences Bldg., Computer Eng. Dept., Univ. of California, Santa Cruz, CA 95064, phone (408) 459-4234, fax (408) 459-3074.

## April 1991

**24th Computer Simulation Conf., Apr. 1-5, New Orleans.** Sponsor: Soc. for Computer Simulation. Contact SCS, Dept. 1991 SMC, PO Box 17900, San Diego, CA 92177, phone (619) 277-3888, fax (619) 277-3930, e-mail mcleod@sdsc.bitnet.

**Workshop on Real-Time Embedded Computing Systems, Apr. 1-5, Bangalore, India.** Sponsor: Assoc. for Advancement of Fault-Tolerant and Autonomous Systems. Contact S. Murugesan, AAFAS, Control Systems Div., ISRO Satellite Centre, Bangalore 560017, India, fax 91 (812) 567-621.

**Φ Dasfaa 91, Second Int'l Symp. on Database Systems for Advanced Applications, Apr. 2-4, Tokyo.** Sponsor: Information Processing Soc. of Japan. Contact Yahiko Kambayashi, Computer Science Dept., Kyushu Univ., 6-10-1 Hakozaki, Higashi Fukuoka 812, Japan, phone 81 (92) 3641-1101, ext. 5407; or Yoshifumi Masunaga, Univ. of Library and Information Science, 1-2 Kasuga, Tsukuba, Ibaraki 305, Japan, phone 81 (298) 52-0511, ext. 340, fax 81 (298) 52-4326, e-mail masunaga@ulis.ac.jp.

**Flairs 91, Florida Artificial Intelligence Research Symp., Apr. 2-5, Cocoa Beach, Fla.** Sponsor: Florida Artificial Intelligence Research Soc. Contact Avelino J. Gonzalez, Computer Eng. Dept., Univ. of Central Florida, Orlando, FL 32816, phone (407) 281-5027, e-mail fdgonzal@ucf1vm.bitnet@cunyvms.cuny.edu.

**Φ SAC 91, 1991 Symp. on Applied Computing, Apr. 3-5, Kansas City, Mo.** Sponsor: Univ. of Missouri — Kansas City. Contact Richard G. Hetherington, Univ. of Missouri, Computer Science Telecommunications Program, 5100 Rockhill Rd., Kansas City, MO 64110-2499, phone (816) 235-2399.

**Third Symp. on Integrated Ferroelectrics, Apr. 3-5, Colorado Springs, Colo.** Contact Conf. Secretary, Microelectronics Research Lab, Univ. of Colorado at Colorado Springs, PO Box 7150, Colorado Springs, CO 80933-7150, phone (719) 593-3488, fax (719) 594-4257.

**Computer Graphics and Education 91, Apr. 4-6, Barcelona, Spain.** Sponsor: Int'l Federation for Information Processing. Contact Steve Cunningham, Computer Science Dept, California State Univ. at Stanislaus, Turlock, CA 95380, phone (209) 667-3176, e-mail rsc@altair.csustan.edu; or Roger Hubbard, Computer Science Dept., Univ. of Manchester, Oxford Road, Manchester M13 9PL, UK, phone

(44) 61-275-6158, e-mail hubbold@uk.ac.man.cs.

**New Directions in Computing: Analytic, Intelligent, and Database Computing, Apr. 7-8, Chicago.** Cosponsors: NASA Ames et al. Contact Janice V. Caudy, Univ. of Illinois at Chicago, Software Tech. Research Center, MC 454, Suite 226, 2201 W. Campbell Park Dr., Chicago, IL 60612-3501, phone (312) 996-5203, fax (312) 413-3029.

**IEEE Infocom 91, Conf. on Computer Comm., Apr. 7-11, Miami, Fla.** Cosponsors: IEEE Computer Soc. and Comm. Soc. Contact N. Shacham, IEEE Infocom 91, SRI Int'l, 333 Ravenswood Ave., Menlo Park, CA 94025, phone (415) 859-5710, e-mail shacham@sri.com.

**1991 IEEE Int'l Conf. on Robotics and Automation, Apr. 7-12, Sacramento, Calif.** Sponsor: IEEE Robotics and Automation Soc. Contact Harry Hayman, Exeter C3037, Boca Raton, FL 33434, phone (407) 483-3037; or Robotics and Automation, PO Box 3216, Silver Spring, MD 20918, phone (301) 434-1990.

**IMS 91, First IEEE Int'l Workshop on Interoperability in Multidatabase Systems, Apr. 8-9, Kyoto, Japan.** Contact Ahmed K. Elmagarmid, Purdue Univ., Computer Sciences Dept., West Lafayette, IN 47907, phone (317) 494-1998; or Yutaka Matsushita, Instrumentation Dept., Keio Univ., Hiyoshi, Yokohama, Japan, phone 81 (44) 63-1141, ext. 3564.

**DCC 91, Data Compression Conf., Apr. 8-10, Snowbird, Utah.** Sponsor: IEEE Computer Soc. Technical Committee on Computer Comm., NASA/CESDIS. Contact Martin Cohn, Computer Science Dept., Brandeis Univ., Waltham, MA 02254, phone (617) 736-2705, fax (617) 736-2741, e-mail marty@cs.brandeis.edu.

**VHDL Users Group Spring Conf., Apr. 8-10, Cincinnati, Ohio.** Contact Conf. Management Services, 407 Chester St., Menlo Park, CA 94025, phone (415) 329-0510, fax (415) 324-3150.

**ASPLOS 4, Fourth Int'l Conf. on Architectural Support for Programming Languages and Operating Systems, Apr. 8-11, Santa Clara, Calif.** Sponsor: ACM. Contact Bob Rau, Hewlett-Packard Labs, 1501 Page Mill Rd., Bldg. 3U, Palo Alto, CA 94304, fax (415) 857-8558, e-mail rau@hplabs.hp.com.

**Seventh Int'l Conf. on Data Eng., Apr. 8-12, Kobe, Japan.** Contact Ming T. (Mike) Liu, Computer and Information Science Dept., Ohio State Univ., 2036 Neil Ave., Columbus, OH 43210-1277, phone (614) 292-1837, e-mail liu@cis.irc.ohio-state.edu; or Data Eng. 91, IEEE Computer Soc., 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013, fax (202) 728-0884.

**Second Int'l Conf. on Computing in Southern Africa, Apr. 8-12, Blantyre,**

Malawi. Sponsor: British Council. Contact E.O. Selim, Univ. of Malawi, Private Bag 303, Chichiri, Blantyre 3, Malawi, phone (265) 670-411, fax (265) 635-088.

**IFIP Working Conf. on Modeling in Computer Graphics, Apr. 8-12, Tokyo.** Sponsor: IFIP TC 5/WG 5.10. Contact Tosiya L. Kunii, Information Science Dept., Faculty of Tokyo, Univ. of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113, Japan, phone 81 (3) 3816-1783, fax 81 (3) 3818-4607, e-mail b39756@tansei.cc.u-tokyo.ac.jp.

**Reliability in Computer Science Conf., Apr. 8-12, Low Tatra Mountains, Czechoslovakia.** Contact Jiri F. Velvsky, EDRC, 1 Tod Campus, West of Scotland, Science Park, Maryhill Rd., Glasgow G20 0XA, UK, phone (041) 946-5020, fax (041) 945-0908.

**Fifth Conf. of the European Chapter of the Assoc. for Computational Linguistics, Apr. 9-11, 1991, Berlin.** Contact Juergen Kunze, Akademie der Wissenschaften, Zentralinstitut fuer Sprachwissenschaft, Prenzlauer Promenade 149-152, Berlin, Germany, phone 37 (2) 4797-153.

**1991 ANSI Public Conf., Seminar, and Workshop, Apr. 9-11, Reston, Va.** Sponsors: Am. Nat'l Standards Inst. et al. Contact External Relations Dept., ANSI, 1430 Broadway, New York, NY 10018.

**ETC 91, 1991 European Test Conf., Apr. 10-12, Munich, Germany.** Sponsor: VDE (Zentralstelle Tagungen und Seminare). Contact Peter Stilke, VDE, Stresemannallee 15, D-6000 Frankfurt 70, Germany, phone 49 (69) 6308-203, fax 49 (69) 6308-273.

**RTA 91, Fourth Int'l Conf. on Rewriting Techniques and Applications, Apr. 10-12, Como, Italy.** Sponsor: State Univ. of Milan. Contact G. Degli Antoni or Marelva Bianchi, Dip. di Scienze Dell' Informazione, Univ. di Milano, Via Milano Moretto da Brescia 9, I-20133 Milano, Italia, phone 39 (02) 7575-201, fax 39 (02) 7611-0556, e-mail gdantoni@imisiam.bitnet.

**Western Educational Computing Workshops, Apr. 11-12, Davis, Calif.** Sponsor: California Educational Computing Consortium. Contact Judah Rosenwald, Extended Education, NAD 153, San Francisco State Univ., 1600 Holloway, San Francisco, CA 94132, phone (415) 338-1212.

**14th IEEE Workshop on Design for Testability, Apr. 15-18, Vail, Colo.** Contact T.W. Williams, IBM, PO Box 1900, Dept. J22/02SR, Boulder, CO 80301-9191, phone (303) 924-7692.

**Ninth IEEE VLSI Test Symp., Apr. 16-18, Atlantic City, N.J.** Cosponsor: IEEE Philadelphia Section. Contact Mukund U. Modi, Naval Air Eng. Center, ATE Software Center, Code: 52514, Bldg. 551, Lakehurst, NJ 08733, home phone (201) 323-7002, office phone (609) 596-0438, fax (201) 323-7445.

**16th Int'l Symp. on Computer Systems, Apr. 16-19, Monterrey, NL, Mexico.** Sponsor: Inst. Tecnológico y de Estudios Superiores de Monterrey. Contact Carlos D. Hinojosa A., Dirección de Carrera ISC, ITESM, Suc. de Correos 'J', CP.64849, Monterrey, NL, Mexico, phone 52 (83) 58-2000, fax 52 (83) 58-8931.

**European Test Conf., Apr. 16-19, Munich, Germany.** Sponsor: Assoc. of German Electrical Eng. Contact Joachim Mucha, Appel str. 9A, Universität, Hannover, D-3000 Hannover 1, Germany.

**Tricomm 91, IEEE Conf. on Comm. Software, Apr. 17-19, Chapel Hill, N.C.** Sponsor: IEEE Comm. Soc. et al. Contact Mary Ducker, CB #3175, Sitterson Hall, Univ. of North Carolina, Chapel Hill, NC 27599-3175, phone (919) 962-1869, fax (919) 962-1799, e-mail ducker@cs.unc.edu.

**PPOPP 91, Third Symp. on Principles and Practice of Parallel Programming, Apr. 21-24, Williamsburg, Va.** Sponsor: ACM SIGPLAN. Contact Dennis Gannon, Computer Science Dept., Indiana Univ., 101 Lindley Hall, Bloomington, IN 47401.

**CHDL 91, 10th Int'l Symp. on Computer Hardware Description Languages and their Applications, Apr. 22-24, Marseille, France.** Cosponsors: Int'l Federation for Information Processing et al. Contact Dominique Borriane, Imag/Artemis, BP 53X, 38041 Grenoble Cedex, France, phone (33) 7651-4604, ext. 5240, fax (33) 7651-9637, e-mail borriane@imag.imag.fr.

**Second European Distributed Memory Computing Conf., Apr. 22-24, Munich, Germany.** Cosponsors: Gesellschaft für Informatik et al. Contact Arndt Bode, Computer Science, Technische Univ. Munich, POB 20-24-20, D-8000 Munich 2, Germany, phone 49 (89) 2105-8240, e-mail bode@infovax.informatik.tu-muenchen.dbp.de.

**KMET 91, Int'l Conf. on Knowledge Modeling and Expertise Transfer, Apr. 22-24, Sophia Antipolis, France.** Cosponsors: Assoc. Francaise pour la Cybernetique Economique et Technique et al. Contact KMET 91, Univ. de Nice, Sophia Antipolis, CNRS, 13S-LISAN, Daniele Herin-Aime, bat. 4, rue A. Einstein, 06560, Valbonne, France, phone (33) 92-94-26-27, fax (33) 92-94-28-98, e-mail dh@cerisi.cerisi.fr.

**Second Eurographics Workshop on Visualization in Scientific Computing, Apr. 22-24, Delft, The Netherlands.** Cosponsors: Delft Univ. of Technology et al. Contact Andrea J.S. Hin, Eurographics VISC Workshop, TU Delft, Faculty of Tech. Math. and Informatics, PO Box 356, 2600 AJ Delft, The Netherlands, phone 31 (15) 783-630, fax 31 (15) 786-522, e-mail andrea@duticg.tudelft.nl.

**Second Int'l Conf. on Systems Integration, Apr. 22-25, Morristown, N.J.** Cosponsors: New Jersey Inst. of Tech. et al. Contact Peter A. Ng, Computer and Information Science Dept., New Jersey Inst. of Tech., University Heights, Newark, NJ 07102, phone

(201) 596-3387, fax (201) 596-5777, e-mail ng\_p@vienna.njit.edu.

**NCGA 91, 1991 Nat'l Computer Graphics Assoc. Conf., Apr. 22-25, Chicago.** Contact NCGA, 2722 Merrilee Dr., Suite 200, Fairfax, VA 22031, phone (800) 225-NCGA or (703) 698-9600, fax (703) 204-4521.

 **Transputing 1991, Apr. 22-26, Sunnyvale, Calif.** Sponsor: Inmos Corp. Contact G.S. Stiles, Electrical Eng. Dept., Utah State Univ., Logan, UT 84322-4120, phone (801) 750-2806, fax (801) 750-3054.

 **CHI 91, 1991 Conf. on Human Factors in Computing Systems, Apr. 27-May 2, New Orleans.** Sponsor: ACM. Contact Toni MacHaffie, 18988 SW Shaw, Aloha, OR 97007, phone (503) 592-1981, fax (503) 591-0120, e-mail machaffie.chi@xerox.com; Keith Butler, Boeing, Advanced Tech. Center, PO Box 24346, MS 7L-64, Seattle, WA 98124, phone (206) 865-3389; or June Davis, 13 Annapolis St., Annapolis, MD 21401, phone (301) 269-6801.

**ECF 91, Eastern Comm. Forum, Apr. 29-May 1, Washington, DC.** Sponsor: Nat'l Eng. Consortium. Contact NEC, 303 E. Wacker Dr., Suite 740, Chicago, IL 60601, phone (312) 938-3500, fax (312) 938-8787.

 **Int'l Conf. on Cognitive Sciences, Apr. 29-May 2, Montreal.** Cosponsors: AFCET et al. Contact Gilles Gauthier, Math. and Computer Science Dept., Univ. of Quebec, PO Box 8888, Station A, Montreal, Que., Canada H3C 3P8, phone (514) 987-8212, fax (514) 987-8477.

 **Fifth Int'l Parallel Processing Symp., Apr. 30-May 2, Anaheim, Calif.** Sponsor: IEEE Computer Soc. Orange County Chapter. Contact Larry H. Canter, Computer Systems Approach, 1140 S. Raymond Ave., Suite B, Fullerton, CA 92631, phone (714) 738-3414, fax (714) 738-3470.

## May 1991

**22nd Pittsburgh Conf. on Modeling and Simulation, May 2-3, Pittsburgh.** Sponsor: Univ. of Pittsburgh. Contact William G. Vogt or Marlin H. Mickle, Modeling and Simulation Conf., 348 Benedum Eng. Hall, Univ. of Pittsburgh, Pittsburgh, PA 15261.

**SID 91, 1991 Int'l Symp., Seminar, and Exhibition, May 6-10, Anaheim, Calif.** Sponsor: Soc. for Information Display. Contact SID, c/o Palisades Inst. for Research Services, 201 Varick St., Suite 1140, New York, NY 10014, phone (212) 620-3371, fax (212) 620-3379.

**IEEE Pacific Rim Conf. on Comm., Computers, and Signal Processing, May 9-10, Victoria, B.C., Canada.** Cosponsors: IEEE Victoria Section, Univ. of Victoria. Contact Technical Program Committee, c/o Pan Agathoklis, Electrical and Computer Eng. Dept., Univ. of Victoria, PO Box 3055, Victoria,

B.C., Canada V8W 3P6, phone (604) 721-8618, fax (604) 721-8676.

**Second Int'l Workshop on Human and Machine Cognition, May 9-11, Pensacola, Fla.** Contact Ken Ford, Inst. for Human and Machine Cognition, Div. of Computer Science, Univ. of West Florida, Pensacola, FL 32514, phone (904) 474-2551, e-mail kford@uwf.bitnet.

 **CBMS 91, Fourth IEEE Symp. on Computer-Based Medical Systems, May 12-14, Baltimore.** Cosponsors: IEEE Computer Soc., IEEE Eng. in Medicine and Biology Soc., and IEEE Baltimore Section. Contact Jeffery C. Lesko, Johns Hopkins Univ., Applied Physics Lab., Bldg. 2-257, Johns Hopkins Rd., Laurel, MD 20723-6099, phone (301) 953-5000, ext. 8057.

**CICC 91, IEEE Custom Integrated Circuits Conf., May 12-15, San Diego, Calif.** Contact Jim Lipman, VLSI Tech., 1109 McKay Dr. MS-32, San Jose, CA 95131, phone (408) 434-7673.

**44th Conf. of the Soc. for Imaging Science and Tech., May 12-17, St. Paul, Minn.** Contact SPSE, 7003 Kilworth Lane, Springfield, VA 22151, phone (703) 642-9090, fax (703) 642-9094.

**Second Eurographics Workshop on Rendering, May 13-15, Barcelona, Spain.** Cosponsors: Univ. Politecnica de Catalunya. Contact Xavier Pueyo, Dept. Llenguatges i Sistemes Informatics, Univ. Politecnica de Catalunya, Av. Diagonal, 647 planta 8, 08028-Barcelona, Spain, phone 34 (3) 401-6667, fax 34 (3) 401-6600, e-mail epueyo@ebrupc51.bitnet or xavier@lsi.upc.es.

 **ICSE 13, 13th Int'l Conf. on Software Eng., May 13-17, Austin, Texas.** Cosponsor: ACM. Contact Barbara Smith, MCC Software Tech. Program, PO Box 200195, Austin, TX 78720, phone (512) 338-3336, fax (512) 338-3899, e-mail basmith@mcc.com; Laszlo A. Belady, MCC, 3500 W. Balcones Center Dr., PO Box 200195, Austin, TX 78759-6509, phone (512) 338-3356; or Bryan Fugate, MCC, 3500 W. Balcones Center Dr., Austin, TX 78759-6509, phone (512) 338-3330.

 **Comp Euro 91, IEEE Int'l Conf. on Advanced Computer Tech., Reliable Systems, and Applications, May 13-17, Bologna, Italy.** Cosponsors: IEEE Region 8 et al. Contact CompEuro 91 Conf. Secretariat, c/o Sercoop, via Crociani 2, 40138 Bologna, Italy, phone 39 (51) 300-811, fax 39 (51) 309-477; or Vito A. Monaco, Dip. di Elettronica Informatica e Sistemistica, Univ. di Bologna, Viale Risorgimento 2, 40136, Bologna, Italy, fax 39 (51) 644-3073.

**Ada-Europe Athens 91 Conf., May 13-17, Athens.** Cosponsors: Ada-Europe et al. Contact Z. Kaplanidis, Zita Tourist Club, 46 Voulis St., GR - 10558 Athens, Greece, phone 30 (1) 323-9744/7, fax 30 (1) 324-1720.

**North Am. Fuzzy Information Processing Soc. Workshop, May 15-17, Columbia, Mo.**

Contact Jim Keller, Electrical and Computer Eng., Univ. of Missouri — Columbia, Columbia, MO 65211, phone (314) 882-7339, fax (314) 882-0397.

**1991 Conf. on Artificial Intelligence in Petroleum Exploration and Production, May 15-17, College Station, Texas.** Contact Technical Program Committee, CAIPEP, Petroleum Eng. Dept., Texas A&M Univ., College Station, TX 77843-3116, phone (409) 845-6950, fax (409) 845-1307.

 **ISSRE 91, Int'l Symp. on Software Reliability Eng., May 17-18, Austin, Texas.** Cosponsors: IEEE Computer Soc. Technical Committee on Software Eng. and the Nat'l Aeronautics and Space Administration. Contact Anneliese von Mayrhauser, Computer Science Dept., Illinois Inst. of Tech., SB236 C 10, West 31st St., Chicago, IL 60616, phone (312) 567-3900, fax (708) 790-1826, e-mail csavm@karl.iit.edu.

**Workshop on Parallel and Distributed Debugging, May 20-21, Santa Cruz, Calif.** Cosponsors: ACM, US Navy Office of Naval Research. Contact Bart Miller, Computer Science Dept., Univ. of Wisconsin, 1210 W. Dayton St., Madison, WI 53706, phone (608) 263-3378, Internet bart@cs.wisc.edu.

 **1991 IEEE Symp. on Research in Security and Privacy, May 20-22, Oakland, Calif.** Sponsor: IEEE Computer Soc. Technical Committee on Security and Privacy. Contact Daniel Schnackenberg, Boeing, MS 9P-64, PO Box 3999, Seattle, WA 98124, phone (206) 657-5595, e-mail schnackenberg@dockmaster.ncsc.mil.

**Second Physical Design Workshop, May 20-22, Laurel Highlands, Pa.** Sponsor: ACM SIGDA. Contact Mary Jane Irwin, Pennsylvania State Univ., Computer Science Dept., University Park, PA 16802, phone (814) 865-1802, e-mail mji@guardian.cs.psu.edu; or Antun Domic, HLO2-3J3, DEC, 77 Reed Rd., Hudson, MA 01749, e-mail domic@cadsys.dec.com.

 **ICDCS 91, 11th Int'l Conf. on Distributed Computing Systems, May 20-24, Arlington, Texas.** Contact Bill D. Carroll, Computer Science Eng. Dept., Univ. of Texas at Arlington, Box 19015, Arlington, TX 76019-0015, phone (817) 273-3785, fax (817) 273-2548, e-mail carroll@evax.utarl.edu.

 **SESAW, Fourth Software Eng. Standards Application Workshop, May 20-24, San Diego, Calif.** Contact Vera V. Edelstein, Nynex, 500 Westchester Ave., White Plains, NY 10604, phone (914) 683-2888.

**EKAW 91, Fifth European Knowledge Acquisition for Knowledge-Based Systems Workshop, May 20-24, Crieff, Scotland.** Contact Duncan Smeed, Computer Science Dept., Univ. of Strathclyde, Livingstone Tower, 26 Richmond St., Glasgow G1 1XH, Scotland, phone (041-552) 4400.

**SCAI 91, Third Scandinavian Conf. on Artificial Intelligence, May 21-24, Roskilde,**

Denmark. Contact Brian Mayoh, Computer Science Dept., Aarhus Univ., Ny Munkegade, Bldg. 540, DK-8000 Aarhus C, Denmark, phone 45 (86) 127188, fax 45 (86) 135725, e-mail brian@daimi.aau.dk.

**Second Int'l Conf. on Algebraic Methodology and Software Tech., May 22-24, Iowa City, Iowa.** Contact Teodor Rus, Computer Science Dept., Univ. of Iowa, Iowa City, IA 52242, phone (319) 335-0694, e-mail rus@herky.cs.uiowa.edu.

**Melecon 91, Fifth Mediterranean Electrotechnical Conf., May 22-24, Ljubljana, Yugoslavia.** Cosponsors: IEEE Region 8 Yugoslavia Section et al. Contact Melecon 91 Secretariat, Fakulteta za elektrotehniko, Trzaska 25, 61001 Ljubljana, Yugoslavia, phone 38 (61) 265-161, fax 38 (61) 264-990.

**Workshop on Interconnections Within High-Speed Digital Systems, May 22-24, Santa Fe, N.M.** Cosponsors: IEEE Comm. Soc. et al. Contact IEEE Lasers and Electro-Optics Soc., 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, phone (908) 562-3896, fax (908) 562-1571.

**Computer Animation 91, May 22-25, Geneva, Switzerland.** Cosponsors: Computer Graphics Soc. Contact Nadia M. Thalmann, Mira Lab CUI, Univ. of Geneva, 12 rue du Lac, CH 1207, Geneva, Switzerland, phone 41 (22) 787-6581, fax 41 (22) 735-3905, e-mail thalmann@uni2a.unige.ch.

**21st Int'l Symp. on Multiple-Valued Logic, May 26-29, Victoria, Canada.** Contact D.M. Miller, Computer Science Dept., Univ. of Victoria, PO Box 1700, Victoria, B.C., Canada, V8W 2Y2, phone (604) 721-7220, fax (604) 721-7292, e-mail dmiller@csr.uvic.cdn.

**ISCA 18, 18th Int'l Symp. on Computer Architecture, May 26-30, Toronto.** Cosponsor: ACM. Contact K.C. Smith, Univ. of Toronto, Electrical Eng. Dept., Toronto, Ont. M5S 1A4, Canada, phone (416) 978-5033.

**ICCI 91, Int'l Conf. on Computing and Information, May 27-29, Ottawa, Canada.** Sponsors: Carleton Univ., Ottawa; Natural Sciences and Eng. Research Council of Canada. Contact Frank Fiala, School of Computer Science, Carleton Univ., Ottawa, Canada K1S 5B6, phone (613) 788-4333, fax (613) 788-4334, e-mail icci@scs.carleton.ca.

**Euro AISIC 91, May 27-31, Paris.** Contact Gabriele Saucier, Inst. Nat'l Polytechnic de Grenoble/CSI, 46, avenue Felix Viallet, 38031 Grenoble Cedex, France, phone 33 (9) 7657-4687.

**Fifth Israel Conf. on Computer Systems and Software Eng., May 28-29, Herzlia, Israel.** Sponsors: IEEE Computer Soc. Israeli Chapter et al. Contact M. Winkur, c/o ORTRA, PO Box 50432, Tel Aviv 61500, Israel, phone 972 (3) 664-825, fax 972 (3) 660-952.

**1991 IEEE Pacific Northwest Test Workshop, May 29-31, Eastsound,**

Wash. Contact Mani Soma, Univ. of Washington, Electrical Eng. Dept., FT-10, Seattle, WA 98195, phone (206) 685-3810, fax (206) 543-3842.

## June 1991

**Workshop on Directions in Automated CAD-Based Vision, June 2-3, Maui, Hawaii.** Contact Linda G. Shapiro, Computer Science and Eng. Dept., FR-35, Univ. of Washington, Seattle, WA 98195, phone (206) 543-2196, fax (206) 543-3842.

**IEA/AIE 91, Fourth Int'l Conf. on Industrial and Eng. Applications of Artificial Intelligence and Expert Systems, June 2-5, Kauai, Hawaii.** Sponsors: ACM et al. Contact Moonis Ali, Univ. of Tennessee Space Inst., MS15, B.H. Goethert Pkwy., Tullahoma, TN 37388-8897, phone (615) 455-0631, ext. 236, fax (615) 454-2354, e-mail alif@utsi1.bitnet.

**11th Int'l Conf. on Decision-Support Systems, June 3-5, Manhattan Beach, Calif.** Sponsor: Inst. for Management Sciences. Contact TIMS, 290 Westminster St., Providence, RI 02903.

**First Golden West Int'l Conf. on Intelligent Systems, June 3-5, Reno, Nev.** Sponsor: Int'l Soc. of Mini and Microcomputers. Contact Carl G. Looney, CS Dept., Univ. of Nevada, Reno, NV 89557, phone (702) 784-6927, e-mail looney@tahoe.unr.edu.

**Fifth Supercomputing Symp., June 3-5, Fredericton, N.B., Canada.** Cosponsors: Canadian Special Interest Group on Supercomputing, Univ. of New Brunswick. Contact Virendra C. Bhavsar or Uday G. Gujar, Faculty of Computer Science, Univ. of New Brunswick, Fredericton, N.B., E3B 5A3, Canada, phone (506) 453-4566, fax (506) 453-3566.

**CVPR 91, IEEE Computer Soc. Conf. on Computer Vision and Pattern Recognition, June 3-7, Lahaina, Maui, Hawaii.** Contact Shahriar Negahdaripour, Electrical Eng. Dept., Univ. of Hawaii at Manoa, 2540 Dole St., Honolulu, HI 96822, e-mail shahriar@wiliki.eng.hawaii.edu.

**20th Mumps Users Group Meeting, June 3-7, New Orleans.** Contact Mumps Users Group, 4321 Hartwick Rd., Suite 100, College Park, MD 20740, phone (301) 779-6555, fax (301) 779-7674.

**Symp. on Solid Modeling Foundations and CAD/CAM Applications, June 5-7, Austin, Texas.** Sponsor: ACM SIGGraph. Contact Joshua Turner, CII 7015, RDRC, Rensselaer Polytechnic Inst., Troy, NY 12180-3590, phone (518) 276-6751, fax (518) 276-2702, e-mail jturner@rdrc.rpi.edu.

**Second Eurographics Workshop on Object-Oriented Graphics, June 5-7, The Nether-**

lands. Sponsor: Dutch Center for Math. and Computer Science (CWI). Contact Marja Hegt, CWI, Kruislaan 413, 1098 SJ Amsterdam, The Netherlands, phone 31 (20) 592-4058, fax 31 (20) 592-4199, e-mail marja@cwi.nl.

**Rapid System Prototyping Workshop, June 10-12, Raleigh, N.C.** Contact Kenneth R. Anderson, Siemens Corp. Research, 755 College Rd. East, Princeton, NJ 08540, phone (609) 734-6550, e-mail kra@siemens.com.

**Parle 91, Conf. on Parallel Architectures and Languages Europe, June 10-13, Eindhoven, The Netherlands.** Cosponsors: Commission of European Communities et al. Contact F. Stoots, Philips Research Labs, PO Box 80.000, 5600 JA Eindhoven, The Netherlands, fax 31 (40) 744-758, e-mail stoots@dooma.prl.philips.nl.

**Summer 1991 Usenix Tech. Conf., June 10-14, Nashville, Tenn.** Contact Usenix Conf. Office, 22672 Lambert St., Suite 613, El Toro, CA 92630, phone (714) 588-8649, fax (714) 588-9706.

**ISCAS 91, 24th IEEE Int'l Symp. on Circuits and Systems, June 11-14, Singapore.** Sponsor: IEEE Circuits and Systems Soc. Contact ISCAS 91 Secretariat, Comm. Int'l Associates, 44/46 Tanjong Pagar Rd., Singapore 0208, phone (65) 226-2823, fax (65) 226-2877.

**SCM 3, Third Int'l Software Configuration Management Workshop, June 12-14, Trondheim, Norway.** Cosponsors: ACM et al. Contact Reidar Conradi, Computer Systems and Telematics Div., Norwegian Inst. of Tech., N-7034 Trondheim, Norway, phone 47 (7) 593-444; or Peter Feiler, Software Eng. Inst., Carnegie Mellon Univ., Pittsburgh, PA 15213-3890, phone (412) 268-7790, e-mail phf@sei.cmu.edu.

**1991 ACM Symp. on Personal and Small Computers, June 12-14, Toronto.** Cosponsors: Nat'l Research Council of Canada et al. Contact Michael Bauer, Computer Science Dept., Middlesex College, Univ. of Western Ontario, London, Ont., Canada N6A 5B7, e-mail bauer@csd.uwo.ca or bauer@uwovax.bitnet.

**BISFAI 91, Bar-Ilan Symp. on the Foundations of Artificial Intelligence, June 16-19, Ramat Gan, Israel.** Sponsor: Bar-Ilan. Contact Ariel Frank, BISFAI 91, Math and Computer Science Dept., Bar-Ilan Univ., Ramat Gan, Israel, e-mail ariel@bimacs.bitnet.

**DAC 91, 28th ACM/IEEE Design Automation Conf., June 17-21, San Francisco.** Contact MP Associates, 7490 Clubhouse Rd., Suite 102, Boulder, CO 80301, phone (303) 530-4333.

**1991 ACM Int'l Conf. on Supercomputing, June 17-21, Cologne, Germany.** Cosponsors: Gesellschaft für Informatik et al. Contact Rüdiger Esser, FKA-ZAM, D-5170 Juelich, Germany, phone 49 (2461) 61-6588, fax 49 (2461) 61-6656, e-mail zdv003@djkfal1.bitnet.

**Eighth Int'l Conf. on Testing Computer Software, June 17-21**, Washington, DC. Sponsor: Data Processing Management Assoc. Educational Foundation. Contact Genevieve Houston-Ludlam, Frontier Technologies, 190 Admiral Cochran Dr., Suite 180, Annapolis, MD 21401, phone (301) 266-8244, fax (301) 224-3840.

**29th Meeting of the Assoc. for Computational Linguistics, June 18-21**, Berkeley, Calif. Contact Don Walker, Bellcore, MRE 2A379, 445 South St., Box 1910, Morristown, NJ 07960-1910, phone (201) 829-4312, e-mail walker@flash.bellcore.com or bellcore!walker.

**CGI 91, Int'l Conf. on Computer Graphics, June 22-28**, Cambridge, Mass. Cosponsors: Computer Graphics Soc., MIT. Contact Barbara Dullea, Ocean Eng. Dept., MIT Rm. 5-435, 77 Massachusetts Ave., Cambridge, MA 02139, fax (617) 253-8125, e-mail barbara@deslab.mit.edu.

**1991 IEEE Int'l Symp. on Information Theory, June 23-28**, Budapest, Hungary. Contact Anthony Ephremides, Electrical Eng. Dept., Univ. of Maryland, College Park, MD 20742, phone (301) 405-3641, arpanet tony@eng.umd.edu.

**ICANN 91, Int'l Conf. on Artificial Neural Networks, June 24-28**, Espoo, Finland. Cosponsors: IEEE Neural Networks Council, Int'l Neural Network Soc. Contact Congress Management Systems, PO Box 151, SF-00141 Helsinki, Finland, phone 358 (0) 175-355, fax 358 (0) 170-122.

 **FTCS 21, 21st Int'l Symp. on Fault-Tolerant Computing, June 25-27**, Montreal. Sponsor: IEEE Computer Soc. Technical Committee on Fault-Tolerant Computing. Contact Vinod K. Agarwal, McGill Univ., Electrical Eng. Dept., 3480 University St., Montreal, Que., Canada H3A 2A7, phone (514) 398-7136, fax (514) 398-4470, e-mail agarwal@spock.ee.mcgill.ca.

**Compass 91, Sixth Conf. on Computer Assurance Systems Integrity, Software Safety, and Process Security, June 25-27**, Gaithersburg, Md. Cosponsors: IEEE Aerospace and Electronics Soc., IEEE Nat'l Capital Area Council. Contact Dolores R. Wallace, Nat'l Inst. of Standards and Tech., Gaithersburg, MD 20899, phone (301) 975-3340, e-mail wallace@swe.ncsl.nist.gov.

**First Int'l Conf. on Artificial Intelligence in Design, June 25-27**, Edinburgh, Scotland. Contact Helen Hodge or Tom Whiting, Butterworth Scientific, Westbury House, Bury Street, Guildford, Surrey, GU2 5BH, UK, phone (0483) 300-966, fax (0483) 301-563.

**Fifth Int'l Conf. on Logic Programming, June 25-28**, Paris. Cosponsors: Assoc. of Logic Programming et al. Contact Inst. Nat'l de Recherche en Informatique et en Automatique (INRIA), Service des Relations Exterieures, Domaine de Voluceau — Rocquencourt, BP 105, 78153 Le Chesnay Cedex, France; phone 33 (1)-39-63-55-00, fax 33 (1) 39-63-56-38, e-mail iclp@minos.inria.fr.

**ICAIL 91, Third Int'l Conf. on Artificial Intelligence and Law, June 25-28**, Oxford, UK. Cosponsors: Soc. for Computer and Law (UK) et al. Contact Carole Hafner, College of Computer Science, Northeastern Univ., Boston, MA 02115, e-mail hafner@corwin.ccs.northeastern.edu; or Richard Susskind, Masons, Solicitors, 30 Aylesbury St., London EC1R 0ER, UK, phone 44 (071) 490-4000, fax 44 (071) 490-2545.

 **Arith 10, 10th Symp. on Computer Arithmetic, June 26-28**, Grenoble, France. Cosponsors: ACM et al. Contact Jean-Michel Muller, Lab. LIP-IMAC, Ens. Lyon, 69364 Lyon Cedex 07, France, phone 33 (72) 72-8229.

**Second Int'l Conf. on Local Communication Systems, June 26-28**, Palma, Spain. Sponsor: Int'l Federation for Information Processing. Contact Ramon Puigjaner, Univ. de les Illes Balears, Carretera de Valldemossa, km. 7.6, 07071 Palma, Spain, phone 34 (71) 207111, fax 34 (71) 758061 or 200741, e-mail dmilan91@ps.uib.es.

**Third Int'l Conf. on Software Eng. and Knowledge Eng., June 27-29**, Skokie, Ill. Sponsors: Knowledge Systems Inst. et al. Contact W.D. Hurley, Computer Science Dept., Alumni Hall, Univ. of Pittsburgh, Pittsburgh, PA 15260, phone (412) 624-8843, e-mail hurley@cs.pitt.edu.

**Sixth IEEE Conf. on Structure in Complexity Theory, June 30-July 3**, Chicago. Contact N. Immerman, Computer and Information Science Dept., Univ. of Massachusetts, Amherst, MA 01003, e-mail immerman@cs.umass.edu.

## July 1991

**IEE Bicentennial Conf. on Computing, July 1-3**, London. Contact Conf. Services, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, UK, phone 44 (71) 240-1871, fax 44 (71) 240-7735.

 **CAR 91, Fifth Int'l Symp. on Computer-Assisted Radiology, July 3-6**, Berlin. Sponsor: Technical Univ. of Berlin. Contact Heinz U. Lemke, Inst. for Technical Computer Science, Sekr CG-FR3-3, Franklinstrasse 28-29, D-1000, Berlin 10, Germany, phone 49 (30) 314-73100; or Michael H. Rhodes, Toshiba America MRI, 280 Utah Ave., South San Francisco, CA 94080, phone (415) 875-2909.

 **Operating Systems of the 90s and Beyond, July 8-12**, Dagstuhl, Germany. Contact Arthur I. Karshmer, New Mexico State Univ., Computer Science Dept., PO Box 30001, Dept. 3CU, Las Cruces, NM 88003-0001, phone (505) 646-2312, fax (505) 646-6218.

**Second Int'l Conf. on Industrial and Applied Math., July 8-12**, Washington, DC. Contact Soc. for Industrial and Applied Math. Conf. Coordinator, Dept. CC0590, 3600 University City Science Center, Philadelphia, PA

19104-2688, phone (215) 382-9800, fax (215) 386-7999, e-mail siamconfs@wharton.upenn.edu.

**ICGA 91, Fourth Int'l Conf. Symp. on Genetic Algorithms, July 13-16**, San Diego, Calif. Contact Richard K. Belew, Computer Science and Eng. Dept., C-014, Univ. of California at San Diego, La Jolla, CA 92093, e-mail rik@cs.ucsd.edu.

**AAAI 91, Ninth Nat'l Conf. on Artificial Intelligence, July 14-19**, Anaheim, Calif. Sponsor: Am. Assoc. for Artificial Intelligence. Contact AAAI 91, 445 Burgess Dr., Menlo Park, CA 94025-3496, phone (415) 328-3123, fax (415) 321-4457, e-mail ncai@aaai.org.

**IAAI 91, Third Conf. on Innovative Applications of Artificial Intelligence, July 15-17**, Anaheim, Calif. Sponsor: Am. Assoc. for Artificial Intelligence. Contact IAAI 91, AAAI, 445 Burgess Dr., Menlo Park, CA 94025-3496, phone (415) 328-3123, fax (415) 321-4457, e-mail iaai@aaai.org.

**Second Int'l Information Research Conf., July 15-18**, Cambridge, UK. Sponsors: British Library Research and Development Dept, Univ. of Pittsburgh. Contact Karen Merry, British Library R&D Dept., 2 Sheraton St., London W1V 4BH, UK, phone 44 (071) 323-7050, fax 44 (071) 323-7251.

**ECOOP 91, Fifth European Conf. on Object-Oriented Programming, July 15-19**, Geneva. Contact Oscar Nierstrasz, Centre Univ. d'Informatique, 12 rue du Lac, CH-1207, Geneva, Switzerland, fax 41 (22) 735-39-05, e-mail oscar@cul.unige.ch; or Karl Lieberherr, Northeastern Univ., College of Computer Science, Cullinane Hall, Boston, MA 02115, phone (617) 437-2077, fax (617) 437-5121, e-mail lieber@corwin.ccs.northeastern.edu.

**JWCC 6, Sixth Joint Workshop on Computer Comm., July 17-19**, Kitakyushu, Fukuoka, Japan. Contact Makoto Takizawa, Information and Systems Eng. Dept., Tokyo Denki Univ., Hatoyama, Saitama 350-03, Japan, phone 81 (492) 96-2911 ext. 2406, fax 81 (492) 96-6185, e-mail taki@takilab.k.dendai.ac.jp.

 **SIGGraph 91, July 30-Aug. 1**, Las Vegas. Sponsor: ACM. Contact Assoc. for Computing Machinery, 11 W. 42nd St., New York, NY 10036, phone (212) 869-7440.

## August 1991

**Fourth Workshop on Computational Learning Theory, Aug. 5-7**, Santa Cruz, Calif. Contact Jean McKnight, Computer and Information Science, Applied Sciences Bldg., Santa Cruz, CA 95064, fax (408) 459-3074, e-mail colt@cis.ucsc.edu.

 **Crypto 91, Aug. 11-15**, Santa Barbara, Calif. Cosponsors: Int'l Assoc. for Cryptologic Research et al. Contact Burt Kaliski, Crypto 91, RSA Data Security, 10

Twin Dolphin Dr., Redwood City, CA 94065, phone (415) 595-8782, fax (415) 595-1873, Internet: burt@rsa.com.

**20th Int'l Conf. on Parallel Processing, Aug. 12-16, St. Charles, Ill.** Sponsor: Pennsylvania State Univ. Contact Tse-yun Feng, Electrical Eng. Bldg. East, Pennsylvania State Univ., University Park, PA 16802, phone (814) 863-1469 or (814) 237-8433.

**1991 Int'l Conf. on Computer Processing of Chinese and Oriental Languages, Aug. 13-16, Taipei, Taiwan.** Cosponsors: Chinese Language Computer Soc. et al. Contact Yaohan Chu, Computer Science Dept., Univ. of Maryland, College Park, MD 20742, phone (301) 405-2667, fax (301) 405-6707, e-mail ychu@cs.umd.edu.

**WADS 91, Workshop on Algorithms and Data Structures, Aug. 14-16, Ottawa, Canada.** Contact WADS 91, School of Computer Science, Carleton Univ., Ottawa, Ont., Canada K1S 5B6, phone (613) 788-4333, fax (613) 788-4334, e-mail wads@scs.carleton.ca.

**Sixth Int'l Conf. CAD/CAM, Robotics, and Factories of the Future, Aug. 19-22, London.** Sponsor: Int'l Soc. for Productivity Enhancement. Contact H. Bera, Mechanical Eng. Dept., South Bank Polytechnic, 103 Borough Rd., London SE1 0AA, UK, phone 011 (91) 81-928-8989, ext. 2095, fax 011 (91) 81-261-9115.

**IJCAI 91, 12th Int'l Joint Conf. on Artificial Intelligence, Aug. 24-30, Sydney, Australia.** Cosponsors: Australian Computer Soc. et al. Contact Barbara J. Grosz, Aiken Computation Lab 20, Harvard Univ., 33 Oxford St., Cambridge, MA 02138, phone (617) 495-3673, fax (617) 495-9837, e-mail grosz@endor.harvard.edu.

**Hot Chips III Symp., Aug. 26-27, Stanford, Calif.** Sponsor: IEEE Computer Soc. Tech. Committee on Microprocessors and Microcomputers. Contact Martin Freeman, Philips Research Labs, Signetics MS 02, 811 E. Arques Ave., Sunnyvale, CA 94086, phone (408) 991-3591, fax (408) 991-4077, e-mail mfreeman@sierra.stanford.edu; or Melissa Anderson, Silicon Graphics, 2011 N. Shoreline Blvd., PO Box 7311, Mountain View, CA 94039-7311, phone (415) 335-1565, fax (415) 965-7651, e-mail mda@sgi.com.

**Tencon 91, 1991 IEEE Region 10 Conf., Aug. 26-30, New Delhi, India.** Contact H.L. Bajaj, B-101 Hillview Apts., Vasant Aihar, New Delhi 110057, India, phone 91 (11) 36-0412, fax 91 (11) 36-1018; or A.L. Lakshminarasimhan, AT&T Bell Labs, 480 Red Hill Rd., No. HR 2E030, Middletown, NJ 07748, phone (201) 615-4524.

**SSD 91, Second Symp. on Large Spatial Databases, Aug. 28-30, Zurich, Switzerland.** Contact Hans-J. Schek, Inst. für Information Systeme, Eth Zentrum, CH-8092 Zurich, Switzerland, phone 41 (1) 254-7240, fax 41 (1) 262-3973, e-mail schek@inf.ethz.ch.

## September 1991

**Eurographics 91, Conf. of the European Assoc. for Computer Graphics, Sept. 2-6, Vienna.** Contact Eurographics 91, c/o Interconvention, Austria Center Vienna, A-1450 Vienna, Austria, phone 43 (1) 2369-2640, fax 43 (1) 2369-648.

**VLDB 91, 17th Int'l Conf. on Very Large Data Bases, Sept. 3-6, Barcelona, Spain.** Sponsors: IEEE Computer Soc. Technical Committee on Data Eng. et al. Contact Guy M. Lohman, IBM Almaden Research Center, Dept. K55, Bldg. 801, 650 Harry Rd., San Jose, CA 95120-6099, Internet lohman@ibm.com, Bitnet lohman@almaden.

**SIGComm 91, ACM Conf. on Communications Applications, Architectures, and Protocols, Sept. 4-6, Zurich, Switzerland.** Contact ACM, 11 W. 42nd St., New York, NY 10036, phone (212) 869-7440.

**Int'l Workshop on Field Programmable Logic and Applications, Sept. 4-6, Oxford, England.** Contact Will Moore, Eng. Science Dept., Univ. of Oxford, Parks Road, Oxford, OX1 3PJ, England, UK, phone 44 (865) 270-373, fax 44 (865) 270-309, e-mail cpdmail@vax.ox.ac.uk.

**Third European Conf. on Electron and Optical-Beam Testing of Integrated Circuits, Sept. 9-11, Como, Italy.** Sponsor: IEEE North Italy Section. Contact Marcello Melgara, CSELT, via Reiss Romoli 274, 10148 Torino, Italy, phone 39 (11) 2169-259, fax 39 (11) 2169-695.

**Third Conf. on Military Robotic Vehicles, Sept. 9-12, Medicine Hat, Alta., Canada.** Cosponsors: Defence Research Establishment Suffield, Alberta Research Council. Contact Dave Mackay, DRES, Box 4000, Medicine Hat, Alta., Canada T1A 8K6, phone (403) 544-4732, fax (403) 544-3388.

**Int'l Conf. on the Performance of Distributed Systems and Integrated Communication Networks, Sept. 10-12, Kyoto, Japan.** Sponsor: Int'l Federation for Information Processing. Contact Yutaka Takahashi, Applied Math and Physics Dept., Faculty of Eng., Kyoto Univ., Kyoto 606, Japan, phone 81 (75) 3753-5493, fax 81 (75) 3761-2437, e-mail yutaka@kuamp.kyoto-u.ac.jp.

**Compsac 91, 15th Int'l Computer Software and Applications Conf., Sept. 11-13, Tokyo.** Cosponsor: Information Processing Soc. of Japan. Contact Stephen S. Yau, Univ. of Florida, CIS Dept., Rm. 301, Gainesville, FL 32611, phone (904) 335-8006 or (904) 392-1212, fax (904) 392-1220, e-mail yau@cis.ufl.edu.

**AI 91, Frontiers in Innovative Computing for the Nuclear Industry, Sept. 15-18, Jackson, Wyo.** Cosponsors: Am. Nuclear Soc. Idaho Section et al. Contact Richard W. Lindsay, Argonne Nat'l Lab, PO Box 2528, Idaho Falls, ID 83403-2528, phone (208) 526-7754, fax (208) 526-7623.

**1991 Electronic Packaging Conf., Sept. 15-19, San Diego, Calif.** Sponsor: Int'l Electronics Packaging Soc. Contact IEPS, 114 N. Hale St., Wheaton, IL 60187-5113, phone (708) 260-1044, fax (708) 260-0867.

**First Int'l Workshop on the Economics of Design and Test, Sept. 23-25, Austin, Texas.** Sponsor: ACM. Contact Magdy Abadir, MCC CAD Program, 3500 W. Balcones Center Dr., Austin, TX 78759, phone (512) 338-3611, fax (512) 338-3600; or A.P. Ambler, Brunel Univ., Dept. of Electrical Eng. and Electronics, Uxbridge, Middx, UB8 3PH, UK, phone (44) 895-74000, fax (44) 895-58728.

**ASIC 91, Fourth IEEE Int'l Application-Specific Integrated Circuits Conf., Sept. 23-27, Rochester, N.Y.** Sponsor: IEEE Rochester Section. Contact Lynne M. Engelbrecht, ASIC 91, 170 Mt. Read Blvd., Rochester, NY 14611, phone (716) 328-2310, fax (716) 436-9370.

**Pacific Rim Int'l Symp. on Fault-Tolerant Systems, Sept. 26-27, Kawasaki, Japan.** Sponsor: Inst. of Electrical, Information, and Comm. Eng. Contact Sachio Naito, Electrical Eng. Dept., Nagaoka Univ. of Tech., 1603-1 Kamitomioka, Nagaoka, Niigata, 940-21, Japan, phone 81 (258) 46-6000, ext. 5110, fax 81 (258) 46-6506.

**IEEE/ACM Int'l Conf. on Developing and Managing Expert System Programs and Projects, Sept. 30-Oct. 2, Washington, DC.** Contact Jerald Feinstein, Mitre, 7325 Colshire Dr., McLean, VA 22102, phone (703) 883-6236, fax (703) 821-0701; or Larry Medsker, Computer Science and Information Systems Dept., American Univ., Washington, DC 20016.

**10th Symp. on Reliable Distributed Systems, Sept. 30-Oct. 2, Pisa, Italy.** Contact Luca Simoncini, IEL-CNR, Via S. Maria 46, 56100 Pisa, Italy, phone 39 (50) 553-159, fax 39 (50) 554-342; or Ozalp Babaoglu, Dip. di Matematica, Univ. di Bologna, Piazza di Porta S. Donato, 5, 40127 Bologna, Italy, phone 39 (51) 354-430, fax 39 (51) 354-490, e-mail ozalp@dm.unibo.it.

**First Int'l Conf. on Document Analysis and Recognition, Sept. 30-Oct. 2, Saint-Malo, France.** Cosponsors: Assoc. Française pour la Cybernetique Economique et Technique et al. Contact Guy Lorette, IRISA-Campus Universitaire de Beaulieu, 35042 Rennes Cedex, France, phone (33) 9936-2000, fax (33) 9938-32.

**First Int'l Conf. of the Austrian Center for Parallel Computation, Sept. 30-Oct. 2, Salzburg, Austria.** Sponsor: ACPIC. Contact R. Schiller, Research Inst. for Software Computation, Univ. of Salzburg, Hellbrunner Str. 34, A-5020 Salzburg, Austria, phone 43 (662) 8044-6701, fax 43 (662) 8044-5010.

## October 1991

**IEEE Workshop on Visual Motion, Oct. 6-9, Princeton, N.J.** Contact Peter Burt, David Sarnoff Research Center, 201 Washington Rd., Princeton, NJ 08540, e-mail burt@vision.sarnoff.com.

**CSEE 91, Fifth Conf. on Software Eng. Education, Oct. 7-8, Pittsburgh.** Sponsor: Software Eng. Inst. Contact James E. Tomayko, SEI, Carnegie Mellon Univ., 4500 Fifth Ave., Pittsburgh, PA 15213-3890, phone (412) 268-6806, fax (412) 268-5758, e-mail jet@sei.cmu.edu.

**11th IEEE Symp. on Mass Storage Systems, Oct. 7-10, Monterey, Calif.** Sponsor: IEEE Computer Soc. Technical Committee on Mass Storage Systems and Technology. Contact Bernard T. O'Lear, NCAR, PO Box 3000, Boulder, CO 80307, phone (303) 497-1268, fax (303) 497-1137.

**First Int'l Conf. on Artificial Intelligence Applications on Wall St., Oct. 9-11, New York City.** Sponsor: Polytechnic Univ., Brooklyn. Contact Mary Bianchi, Polytechnic Univ., 333 Jay St., Brooklyn NY 11201, phone (718) 260-3360, fax (718) 260-3136.

**Int'l Workshop on Visual Languages, Oct. 9-11, Kobe, Japan.** Cosponsors: Hiroshima Univ., Univ. of Pittsburgh. Contact Shi-Kuo Chang, Computer Science Dept., Univ. of Pittsburgh, Pittsburgh, PA 15260, phone (412) 624-8423, fax (412) 624-8465.

**Workshop on Experimental Distributed Systems, Oct. 12, Huntsville, Ala.** Contact Raif M. Yanney, TRW, 1 Space Park, DH2/2328, Redondo Beach, CA 90278, phone (213) 764-6033.

**RIDT 91, Second Int'l Workshop on Raster Imaging and Digital Typography, Oct. 14-15, Boston.** Sponsor: Univ. of Massachusetts. Contact Robert A. Morris, Math. and Computer Science Dept., Univ. of Massachusetts at Boston, Harbor Campus, Boston, MA 02125-3393, phone (617) 287-6466, e-mail ridt91-request@cs.umb.edu.

**ICCD 91, IEEE Int'l Conf. Symp. on Computer Design, Oct. 14-16, Cambridge, Mass.** Cosponsors: IEEE Computer Soc. and IEEE Circuits and Systems Soc. Contact ICCD 91, IEEE Computer Soc., 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**16th Conf. on Local Computer Networks, Oct. 14-17, Minneapolis, Minn.** Cosponsor: IEEE Computer Soc. Technical Committee on Computer Comm. Contact James F. Mollenauer, 16th LCN Conf., Artel Communications, 22 Kane Industrial Dr., Hudson, MA 01749, phone (508) 562-2100, fax (508) 562-6942.

**Conf. on Software Maintenance, Oct. 14-17, Sorrento, Italy.** Cosponsor: IEEE. Contact Vaclav Rajlich, Computer Science Dept., Wayne State Univ., Detroit, MI

48202, phone (313) 577-5423, fax (313) 577-6868, e-mail vtr@cs.wayne.edu; John Munson, Computer Science Dept., Univ. of West Florida, Pensacola, FL 32514; or Malcolm Munro, Centre for Software Maintenance, Univ. of Durham, Durham, DH1 3LE, England, phone 44 (091) 374-2634, e-mail malcolm.munro@uk.ac.durham.

**Visualization 91, Oct. 22-25, San Diego, Calif.** Sponsor: IEEE Computer Soc. Technical Committee on Computer Graphics. Contact Bruce Brown, Oracle, 500 Oracle Pkwy., MD 40P12, Redwood Shores, CA 94065, phone (415) 726-0983, fax (415) 506-7200; or Gregory M. Nielson, Computer Science Dept., Arizona State Univ., Rural Road and University, Tempe, AZ 85287-5406, phone (602) 965-2785.

**Sixth Int'l Workshop on Software Specification and Design, Oct. 25-26, Como, Italy.** Contact C. Ghezzi, Dip. di Elettronica, Politecnico di Milano, Piazza Leonardo Da Vinci 32, 20133 Milano, Italia, e-mail relett24@imipoli.bitnet; or Jean-Pierre Finance, CRIN, Campus Scientifique, BP 239 54000 Nancy, France, e-mail finance@loria.crin.fr.

**ILPS 91, Int'l Logic Programming Symp., Oct. 28-31, San Diego, Calif.** Sponsor: Assoc. of Logic Programming. Contact Kenneth Kahn or Vijay Saraswat, Xerox PARC, 3333 Coyote Hill Rd., Palo Alto, CA 94304, Kahn's phone (415) 494-4390, Saraswat's phone (415) 494-4747, fax (415) 494-4334, e-mail ilps91@parc.xerox.com.

**ITC 91, Int'l Test Conf., Oct. 28-Nov. 1, Nashville, Tenn.** Cosponsor: IEEE Philadelphia Section. Contact Doris Thomas, PO Box 264, Mt. Freedom, NJ 07970, phone (201) 895-5260, fax (201) 896-7265; or IEEE Computer Soc., 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

## November 1991

**TAI 91, Third IEEE Computer Soc. Conf. on Tools for Artificial Intelligence, Nov. 10-13, San Jose, Calif.** Contact Benjamin Wah, Coordinated Science Lab, MC 228, Univ. of Illinois, 1101 W. Springfield Ave., Urbana, IL 61801-3082, phone (217) 333-3516, fax (217) 244-1764, e-mail wah%aquinas@cso.uiuc.edu; or Nikolaus G. Bourbakis, 4138 Moonflower Ct., San Jose, CA 95135, phone (408) 270-3455.

**ICCAD 91, IEEE Int'l Conf. on Computer-Aided Design, Nov. 11-14, Santa Clara, Calif.** Cosponsor: IEEE Circuits and Systems Soc. Contact ICCAD 91 Secretary, MP Associates, 7490 Clubhouse Rd., Suite 102, Boulder, CO 80301, phone (303) 530-4562.

**Supercomputing 91, Nov. 18-22, Albuquerque, N.M.** Cosponsor: ACM. Contact Raymond L. Elliott, Computing and

Comm. Div., MS B260, Los Alamos Nat'l Lab, Los Alamos, NM 87545, phone (505) 667-1449, fax (505) 665-4361, e-mail rle@lanl.gov; or Supercomputing 91, IEEE Computer Soc., 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.

**Third Int'l Symp. on Parallel and Distributed Processing, Nov. 26-30, Dallas.** Contact Behrooz Shirazi, Univ. of Texas at Arlington, Computer Science Eng. Dept., Box 19015, Arlington, TX 76019-0015, phone (817) 273-3605, fax (817) 273-2548, e-mail shirazi@evax.utarl.edu.

## December 1991

**12th IEEE Symp. on Real-Time Systems, Dec. 3-6, San Antonio, Texas.** Sponsor: IEEE Computer Soc. Tech. Committee on Real-Time Computing. Contact Jane S.W. Liu, Computer Science Dept., Univ. of Illinois, 1304 W. Springfield Ave., Urbana, IL 61801, phone (217) 333-0135, e-mail janeliu@cs.uiuc.edu.

**Int'l Conf. on Parallel and Distributed Information Systems, Dec. 4-6, Miami Beach, Fla.** Cosponsors: IEEE Computer Soc. et al. Contact Amit Sheth, Bellcore, 1J-210, 444 Hoes Ln., Piscataway, NJ 08854, phone (908) 699-3300, fax (908) 699-9011, e-mail amit@ctt.bellcore.com.

**1991 Winter Simulation Conf., Dec. 8-11, Phoenix, Ariz.** Sponsor: ACM. Contact Robert Crain, Wolverine Software, 4115 Annandale Rd., Suite 200, Annandale, VA 22003.

**World Congress on Expert Systems, Dec. 16-19, Orlando, Fla.** Cosponsors: Int'l Assoc. of Knowledge Engineers et al. Contact World Congress on Expert Systems, c/o Congress Secretariat, Congrex (USA), Inc., 7315 Wisconsin Ave., Suite 404E, Bethesda, MD 20814, phone (301) 469-3355, fax (301) 469-3360.

## January 1992

**Hawaii Int'l Conf. on Systems Sciences, Jan. 7-10, Koloa, Hawaii.** Cosponsors: IEEE, ACM. Contact Luqi, Computer Science Dept, Naval Postgraduate School, Monterey, CA 93940, phone (408) 646-2468.

## February 1992

**Compcon Spring 92, Feb. 24-28, San Francisco.** Contact Compcon Spring 92, IEEE Computer Soc., 1730 Massachusetts Ave. NW, Washington, DC 20036-1903, phone (202) 371-1013.



# ADVANCE ANNOUNCEMENT

## IEEE Computer Society Conference on Computer Vision and Pattern Recognition

Maui Marriott on Kaanapali Beach  
Lahaina, Maui, Hawaii  
June 3-6, 1991

### CVPR '91 REGISTRATION FORM

Return registration form to: CVPR '91 Registration, IEEE Computer Society, 1730 Massachusetts Avenue, N.W., Washington, DC 20036-1903, (202)371-1013, FAX (202)728-0884

#### Please type or print

Name \_\_\_\_\_  
Last/Family First Middle Initial Badge Name  
Company/University \_\_\_\_\_  
Address/Mailstop \_\_\_\_\_  
City/State/Zip/Country \_\_\_\_\_  
Daytime Phone Number \_\_\_\_\_ Fax Number \_\_\_\_\_ IEEE/CS Membership Number \_\_\_\_\_

#### Tutorials--Monday June 2, 1991

- ☐ 1: Task-Based Vision, K. Ikeuchi and C. Thorpe (8:30 a.m.-5:30 p.m.)  
☐ 2: Architectures for Computer Vision, J. Sanz and B. Dom (8:30 a.m.-5:30 p.m.)  
☐ 3: Psychophysics and Computer Vision, H. Bulthoff (8:30 a.m.-12:30 p.m.)  
☐ 4: Computational Geometry and Computer Vision, G. Toussaint (1:30-5:30 p.m.)

#### Tutorial Registration--Price is per Tutorial

Advance (Until 5/3/91) Late/On Site (After 5/3/91)

##### Full-day Tutorials

- ☐ Member: \$190 ☐ Member: \$230  
☐ Nonmember: \$240 ☐ Member: \$290

##### Half-day Tutorials

- ☐ Member: \$120 ☐ Member \$145  
☐ Nonmember: \$150 ☐ Nonmember \$185

Conference registration fees include the proceedings and the Hawaiian Luau Dinner/Show for non-student registrants (Luau tickets will be available for students or companions).

Written requests for refunds must be received in the IEEE Computer Society office no later than May 3, 1991. Refunds are subject to a \$50 processing fee. All no show registrations will be billed in full. Students are required to show current picture ID cards at the time of registration. Registrations after May 17, 1991 will be accepted on-site only.

#### Conference Registration

Advance (Until 5/3/91) Late/On Site (After 5/3/91)

- ☐ Member: \$265 ☐ Member \$320  
☐ Nonmember: \$335 ☐ Nonmember \$400  
☐ Student: \$120 ☐ Student \$130

Total Enclosed \$ \_\_\_\_\_

Payment must be enclosed. Please make checks payable to IEEE Computer Society. All payments must be in U.S. dollars, drawn on U.S. banks.

#### Method of payment accepted:

- ☐ Personal Check ☐ Company Check ☐ Traveler's Check ☐ VISA  
☐ MasterCard ☐ American Express ☐ Purchase Order  
(must accompany registration form)

Cardholder Name \_\_\_\_\_ Signature \_\_\_\_\_  
Card Number \_\_\_\_\_ Expiration Date \_\_\_\_\_

### CVPR HOTEL REGISTRATION FORM

Please mail or fax this form with your payment to: Maui Marriott on Kaanapali Beach, Lahaina, Maui, HI 96761, (808)667-1200, FAX (808)661-8575

#### Rates

\$110 single or double accomodation, \$25 per additional person

- ☐ Single ☐ Double ☐ Other: \_\_\_\_\_ ☐ Smoking room ☐ Non-smoking room

Name \_\_\_\_\_  
Company/University \_\_\_\_\_  
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#### Method of Payment:

- ☐ Check ☐ American Express ☐ VISA ☐ MasterCard ☐ Diners Club ☐ Carte Blanche

Cardholder Name \_\_\_\_\_ Signature \_\_\_\_\_  
Card Number \_\_\_\_\_ Expiration Date \_\_\_\_\_

All reservations must be received by the hotel before May 3, 1991. Reservations received after this date will be accepted on a space available basis only. A one-night deposit is required within 10 days of the reservation date. All rates are subject to a 9.167% occupancy tax. Please be advised that the hotel check-in time is 4 p.m. and check-out time is 12 noon.

### AIRLINE AND CAR RENTAL INFORMATION

Conference Attendees will receive 5% off the lowest available discounted fare or 40% off the regular coach fares on United and American Airlines (domestic flights only). Special daily and weekly rental car rates from a week prior to a week after the conference dates are available from Hertz Rent-a-Car.

For airline and car rental information contact:  
IEEE Computer Society Conference Department,  
(202)371-1013).

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# CAREER OPPORTUNITIES

**RATES:** \$12.00 per line, (ten lines minimum). Average five typeset words per line, eight lines per column inch. Add \$10 for box number. Send copy at least one month prior to publication date to: **Marian B. Tibayan, Classified Advertising, COMPUTER Magazine, 10662 Los Vaqueros Circle, PO Box 3014, Los Alamitos, CA 90720-1264; (714) 821-8380; fax (714) 821-4010.**

In order to conform to the Age Discrimination in Employment Act and to discourage age discrimination, *COMPUTER* may reject any advertisement containing any of these phrases or similar ones: "...recent college grads...", "...1-4 years maximum experience...", "...up to 5 years experience," or "...10 years maximum experience." *COMPUTER* reserves the right to append to any advertisement, without specific notice to the advertiser, "Experience ranges are suggested minimum requirements, not maximums." *COMPUTER* assumes that, since advertisers have been notified of this policy in advance, they agree that any experience requirements, whether stated as ranges or otherwise, will be construed by the reader as minimum requirements only.

## INFORMATION WANTED

### REQUEST FOR INFORMATION (RFI) COMPUTERIZED TICKET ISSUANCE EQUIPMENT

The New York City Department of Transportation requests information regarding the available technology in the field of computerized hand-held ticket issuance and data recording equipment for parking violations. Based on responses due May 10, 1991, the Department may begin a procurement process.

Requests for RFI package should be directed to:

RFI Coordinator  
NYC Department of Transportation  
1 Centre Street, Room 1307  
New York, N.Y. 10007

### THE OHIO STATE UNIVERSITY Dean of The College of Engineering

The Ohio State University invites applications and nominations for the position of Dean of the College of Engineering.

The Dean will lead a distinguished 260-person faculty, serving 4,500 undergraduate and 1,400 graduate students in 16 academic

units. The Dean will administer a total budget of \$90,000,000, including the sixth largest engineering college research budget in the United States, and will have the support of 30,500 College of Engineering alumni. The candidate should be a recognized leader in administration, research and teaching. The Dean will be a key member of the university leadership and will be expected to contribute to the broad academic and cultural missions of the entire university.

The position will be available July 1, 1991. The Ohio State University is an equal opportunity/affirmative action employer, and the candidate must be committed to these principles. The Search Committee will accept and review applications until the position is filled.

Send applications and nominations, including curriculum vitae and the names of three references to Professor Leon Peters, Jr., Chair, Search Committee for the Dean of the College of Engineering, Department of Electrical Engineering, The Ohio State University, 2015 Neil Avenue, Columbus, OH 43210.

### THE UNIVERSITY OF ILLINOIS Department of Electrical and Computer Engineering

The Department of Electrical and Computer Engineering invites applications for several tenure-track and tenured faculty positions. Applicants must have an earned Ph.D., outstanding academic credentials, and an ability to teach effectively at both the graduate and undergraduate levels. Selected candidates will be expected to initiate and carry out independent research and to perform academic duties associated with our B.S., M.S., and Ph.D. programs. Since the department is very large, each year several vacancies are filled. A continuing search is conducted throughout the year to fill open positions. All candidates judged as qualified for a position will be interviewed. Salary open, based on qualifications. Starting date is negotiable. The department has one of the largest programs in the United States granting approximately 400 B.S., 100 M.S., and 65 Ph.D. degrees annually. The department is recruiting faculty in all areas of computer engineering. Current research interests of our computer engineering faculty include computer architecture, design complexity and theory of computation, high performance and reliable computing, knowledge engineering, parallel and distributed processing, performance evaluation, robotics and computer vision, and VLSI design.

Send resume, with references and a list of publications, to: T.N. Trick, Faculty Search Committee, University of Illinois, Department of Electrical and Computer Engineering, 1406 West Green Street, Urbana, IL 61801. Telephone: (217) 333-2301.

The University of Illinois is an equal opportunity/affirmative action employer.

### NJIT Faculty: Computer and Information Science

NJIT seeks assistant, associate and full professors for Spring/Fall 1991 in distributed computing including computer architecture, operating systems, data communications and networking, realtime computing and fault tolerance, software development including compiling, computer graphics, office automation, data management systems, information management systems, cognitive science, and computational linguistics; computer graphics and computer visions and other areas. Qualifications: Ph.D. in computer science or closely related field required; senior level applicants must have proven research and funding record.

The department offers B.S., B.A., M.S. and Ph.D. in computer science. Computing facilities include the \$30 million Information Technologies Building with VAX 6400, VAX 8530, IBM 4361, SUN workstations, Symbolics machines, TI Explorers and graphic systems. Send resume and names of three references to: Personnel Box CIS.

NJIT is the technological university of New Jersey with nearly 8,000 students enrolled in Newark College of Engineering, the School of Architecture, the College of Science and Liberal Arts and the School of Industrial Management.

NJIT does not discriminate on the basis of sex, race, color, handicap, religion, national or ethnic origin or age in employment.

NEW JERSEY INSTITUTE OF  
TECHNOLOGY  
University Heights  
Newark, NJ 07102

### OREGON STATE UNIVERSITY Department of Computer Science

The Department of Computer Science invites applicants for tenure-track positions for Assistant, Associate, and Full Professorships. Specialization in computer graphics or software engineering is desirable, but all qualified applicants will be considered. Applicants should have completed or expect to complete all requirements for a Ph.D. in computer science or a closely related field and should have demonstrated research and teaching potential. Candidates for senior positions should have established research reputations. Review of applications will begin November 1, 1990, and will continue until the positions are filled. Please send vita, statement of research interests and plans, and three letters of reference to: Walter G. Rudd, Chairman, Department of Computer Science, Oregon State University, Corvallis, OR 97331.

Oregon State University is an equal opportunity affirmative action employer and complies with Section 504 of the Rehabilitation Act of 1973. OSU has a policy of being responsive to the needs of dual-career couples.

## INFORMATION SCIENTIST

Information Scientist, real estate research and information, 40 hours per week, \$36,000 per year. Design information system to provide specific data from computer storage using data processing principles, mathematics and computer capabilities in an on-line environment. Select appropriate database for map engine in an on-line environment. Develop dbVista versus proprietary database for map storage. Select database appropriate for storage of map file on CD ROM. Create set of rules required for storage of map data to ensure acceptable response time in an on-line environment. Understand constraints of CD ROM media and Map Engine in an on-line environment. Analyze and develop procedures for updating map database stored on CD ROM for use in an on-line environment. Implement these procedures in design. Create algorithm for displaying a 3-dimensional view of ground surface. Assume input to be in Digital Line Graph Level 3 format from the USGS office, and define user interface. Code in 'C.' Integrate function with our mapping modules in an on-line environment. Document design. Create graphics monitor program for displaying windows on a computer screen, permitting other calling programs to perform editing and displaying functions in an on-line environment. Define interfaces and calling protocols to these other programs. Identify need for specific modular functions to minimize redundancy and increase reliability. Code in 'C.' Document design. Create algorithms for compressing and decompressing raster files. Write algorithms in 'C.' Document design. Assist in integration of programs with other mapping modules in an on-line environment. Minimum requirements: M.S. in Computer Science, 6 months in the job offered or 6 months as an Information Systems Programmer with on-line experience. Apply at the Texas Employment Commission, Dallas, Texas, or send resume to the Texas Employment Commission, TEC Building, Austin, Texas 78778, J.O. 6122942. Ad Paid by an Equal Employment Opportunity Employer.

## CARNEGIE MELLON UNIVERSITY School of Computer Science

The Introductory Programming Group within the School of Computer Science has more than one non-tenure track, full-time teaching position available July 1991. The main duty is the teaching of undergraduate programming courses. Our computing facilities include 50 Macintosh computers, several servers, printers, and a LAN. Most courses use Pascal as a support language.

Applicants for the positions must have a M.S. in Computer Science (or related field), and strong academic credentials or practical experience. Knowledge of Pascal and Macintosh is preferred. Qualified applicants should send a letter of application, resume, and three letters of recommendation to: Jacobo Carrasquel, Carnegie Mellon, School of Computer Science, Pittsburgh, PA, 15213.

Carnegie Mellon is an Equal Opportunity/Affirmative Action Employer. Women and minorities are especially encouraged to apply.

## CONCORDIA UNIVERSITY Centre for Pattern Recognition and Machine Intelligence (CENPARMI)

CENPARMI is a new centre established in the Faculty of Engineering and Computer Science at Concordia University to foster close collaborations among active researchers in Pattern Recognition and Machine Intelligence and the industrial sector. Presently 12 faculty members and 50 research staff and graduate students are associated with the centre.

CENPARMI invites applications for two post-doctoral and research positions in verification and validation of expert systems, automatic document processing and understanding, and machine learning applied to pattern recognition, starting Spring or Summer 1991. Candidates should have experience in one of the above areas. Send resume, reprints of publications, and the names of three or more references as soon as possible and before April 30, 1991 to Dr. C.Y. Suen, Director, Centre for Pattern Recognition and Machine Intelligence, Concordia University, 1455 de Maisonneuve Boulevard West, Montreal, Quebec H3G 1M8, Canada.

In accordance with Canadian Immigration requirements, this advertisement is directed to Canadian citizens and permanent residents. However, foreign applicants are also encouraged to apply.

## WASHINGTON UNIVERSITY

Washington University in St. Louis seeks qualified candidates for the position of Professor and Chair of the Department of Computer Science, with a desired starting date of July 1, 1991. We are interested in candidates with a strong research record, with a dedication to excellence in undergraduate and graduate education and with a demonstrated potential for administration and leadership.

The Department has an excellent undergraduate program as well as a strong and expanding graduate program. The primary research concentrations are in distributed systems, advanced communication networks and intelligent computer systems with an emphasis on visualization as a tool in each case. The Department plans to continue building on these areas of strength as well as expanding into new areas. There are 15 regular faculty in the Department and 85 graduate students, as well as an excellent technical support staff and a large pool of affiliate faculty. Departmental laboratory facilities are very good and include a visualization laboratory, a systems prototyping lab, an NCUBE parallel computer, a variety of compute servers and ubiquitous workstations.

Washington University has a longstanding commitment to the principle that all candidates should be afforded equal opportunity regardless of age, race, sex or physical disability. Candidates must send a curriculum vitae and a list of references to: Professor C.I. Byrnes, Search Committee for the Computer Science Chair, Campus Box 1040, Washington University, One Brookings Drive, St. Louis, MO 63130.

## SOFTWARE ENGINEER

Work with team creating next generation development environment for real-time expert systems. Perform primary coding for project, learn internals of proprietary operating system and serve as in-house technical resource. Strong engineering and CS background. C, 6502 assembly, prior Mao application development experience required.

UMECORP is an AI firm offering the flexibility of a small company with the excitement of a growing start-up environment. Benefits include medical/dental and strong stock incentives. Send resume and salary history to:

Personnel Manager  
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73 Digital Dr., MS/IC391  
Novato, CA 94949

## UNIVERSITY OF CALIFORNIA LOS ANGELES

Applications are invited for a tenure-track position in the UCLA Computer Science Department. Both junior and senior level applicants are solicited. A doctoral degree is required along with a demonstrated commitment to teaching and outstanding research. We are especially interested in candidates whose research is in the area of computer systems (hardware or software). Please send a resume, a subset of your best papers, and the names of four references to:

Professor Wesley Chu, Chair  
Computer Science Department (Recruiting)  
3732 Boelter Hall  
University of California  
Los Angeles, CA 90024  
The University of California is an Equal Opportunity, Affirmative Action Employer.

## DUKE UNIVERSITY Department of Computer Science

Applications are invited for a possible tenure-track position in the area of Scientific Computing at the rank of Assistant Professor, beginning September 1991.

The Department has major research efforts in scientific computing with emphasis on numerical linear algebra, the solution of PDEs, and VLSI simulation; artificial intelligence, particularly in the areas of logic programming, natural language interface, and search methodologies; theory and algorithms with emphasis on parallel and randomized algorithms; and computer systems with emphasis on systems performance, communications, and computer architectures.

Applicants should include a curriculum vitae, a list of publications, a few most important publications and a list of references. These should be sent by March 31, 1991 to:

Professor Donald J. Rose, Chairman  
Department of Computer Science  
Duke University  
Durham, NC 27706

Duke University is an affirmative action, equal opportunity employer.

**THE WICHITA STATE UNIVERSITY  
Instructor/Research Associate  
Computer Science Department**

Applications are invited for the temporary position of instructor/research associate in the Computer Science Department. The closing date is April 5, 1991. The term of employment for this position is the academic year 1991-1992 beginning August 18, with possible extension to six years.

Responsibilities include teaching undergraduate computer science courses and assisting in research on machine discovery.

Qualifications include M.S. degree in Computer Science, demonstrated aptitude in teaching undergraduate computer science courses, knowledge of and experience in artificial intelligence using Lisp and C languages, with particular experience in machine discovery and learning. In addition, knowledge and work experience in LAN hardware and software as well as experience in developing communication protocols in distributed computer systems are essential. Preference will be given to candidates whose interests, knowledge, and skills most closely fit the current departmental research in machine discovery.

Applicants should send a cover letter stating their teaching and research interests and experience, a resume, copies of transcripts, and names and addresses of three professional references, at least one of whom can assess the candidate's teaching and research qualifications to: Dr. Raj Sunderraman, Chairman, Faculty Search Committee, Computer Science Department, The Wichita State University, Wichita, KS 67208, (316) 689-3156, fax: (316) 689-3770, sunderraman@twsvax.bitnet. The Wichita State University is an Equal Opportunity/Affirmative Action Employer.

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**NATIONAL RADIO  
ASTRONOMY OBSERVATORY  
VLA Computer Division  
Attention: Ina Cole, Personnel Office**

The National Radio Astronomy Observatory seeks a senior scientific programmer/analyst to join a small team responsible for designing a new data calibration and imaging system which will replace the widely distributed AIPS package. The successful candidate will have extensive knowledge of and experience with database design technology. Candidates should have at least an MS or equivalent in computer science, with at least five years of programming experience. Candidates should also be experienced with graphics and visualization of scientific data. Experience of programming in a UNIX environment is required. Experience with the C and FORTRAN programming languages would be an advantage, as would some knowledge of astronomy.

The National Radio Astronomy Observatory is a federally-funded research organization which designs, builds, and operates advanced radio astronomy instruments for research in astronomy. These instruments include the Very Large Array (VLA), an array of 27 antennas located near Socorro, N.M., and the Very Long Baseline

Array (VLBA), an array of 10 antennas, currently under construction, which are located at various sites throughout the continental U.S.A., Hawaii, and U.S. Virgin Islands. These facilities, and others, are available to all researchers without charge, and are used by over 150 individuals representing over 50 separate proposals per month.

One of the responsibilities of the N.R.A.O. is to provide the necessary software for reduction of the vast quantities of data produced by these arrays, and by individual antennas. This software must be easy to use, easy to modify, and portable since much of the data reduction and analysis is done by individuals at their home institutions. To satisfy these needs, the observatory developed the Astronomical Imaging Processing System (AIPS), which is currently installed at about 200 sites throughout the world. However this software package, which was initially designed in the late 1970s, has become too large and unwieldy for efficient maintenance. The Observatory has therefore decided to assemble a small team to design and implement a new software package. We are seeking a capable individual to join this team.

This position is located at the Array Operations Center in Socorro, New Mexico. Applications must be received by May 1, 1991, P.O. Box O, Socorro, NM 87801.

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**TUSKEGEE UNIVERSITY**

Applications are invited for a faculty position in Computer Science Department, in Information System. Rank and salary dependent upon qualifications. A Ph.D. in Computer Science, or Information Systems, or a related area with sufficient background in Information Systems is required.

Facilities include VAX-11/750, VAX-11/780, IBM 4381, IPSC/1. Micro VAX-11, AT&T's 3B2/400, 3B2/500, 3B2/600 machines and many Microcomputers, as well as terminals.

Send Vita and Transcripts to Dr. H.N. Narang, Head, Computer Science Department, Tuskegee University, Tuskegee, AL 36088.

AN EQUAL OPPORTUNITY/AFFIRMATIVE ACTION EMPLOYER.

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**THE GEORGE WASHINGTON  
UNIVERSITY  
Electrical Engineering and  
Computer Science  
Tenure-Track Faculty Positions**

Tenure-track faculty positions at the assistant, associate, and full professor rank are available commencing Fall Semester 1991, in the Department of Electrical Engineering and Computer Science of the School of Engineering and Applied Science.

Applicants are sought to conduct research and teach in the areas of communications, data communications/computer networks, telecommunications, computer graphics, analog electronics/VLSI, and computer engineering. Applications from other highly-qualified individuals are encouraged. Candidates should have an earned doctorate and research experience with an interest in

both teaching and research. Ability to attract funded research is valued.

The George Washington University main campus is located in the center of Washington, D.C. A research and graduate teaching campus, set in a major research park in suburban Virginia near Washington-Dulles Airport, will open in September 1991. Substantial equipment and student stipends are available for faculty capable of establishing government and industry-supported research projects at the new campus. Off-campus research/education programs at NASA-Goddard Space Flight Center and Melpar E-Systems provide additional opportunities for collaborative work with local industry and government laboratories.

The metropolitan Washington area has the second largest concentration of research and development activity in the United States, creating a continuing demand for rigorously-trained engineers and many research opportunities. The department has 40 full-time faculty, accredited electrical engineering, computer engineering, and computer science degree programs, a large graduate and undergraduate student body, and a substantial research budget. Current projects include computer graphics, computer security, data transmission standards and compression, fast packet switching, network topologies, image processing, intelligent user interfaces, laser shields, MHD plants, magnetic devices, medical imaging, parallel processing architectures and scheduling, multipath fading and encryption, remote sensing, robot control, space-based radar, and special-purpose VLSI designs.

Send curriculum vita, list of publications and references to:

Chairman, Faculty Search Committee  
Department of Electrical Engineering and  
Computer Science

School of Engineering and Applied Science  
The George Washington University  
Washington, D.C. 20052

The George Washington University is an affirmative action/equal opportunity employer.

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**UNIVERSITY OF MIAMI  
Department of Electrical and  
Computer Engineering**

The Department of Electrical and Computer Engineering invites applications for a tenure-track faculty position in computer engineering at the Assistant/Associate Professor level. Preferred areas of interest are operating systems, software engineering and database systems.

Qualifications include a Ph.D. degree in computer science or computer engineering, and the ability of initiating research projects, attracting external funding, and teaching undergraduate and graduate courses. Salary will be commensurate with rank and experience.

The University is located in Coral Gables, a suburb of Miami, Florida. Applications should be sent with the names of three references to: Dr. Tzay Y. Young, Acting Chairman, University of Miami, Dept. of Electrical and Computer Engineering, P.O. Box 248294, Coral Gables, Florida 33124.

The University of Miami is an equal opportunity/affirmative action employer.

**FLORIDA INSTITUTE OF  
TECHNOLOGY**  
Professor of Computer Science

Applications are invited at all levels in the Department of Computer Science, for appointment commencing Fall 1991.

A Ph.D. in Computer Science or a closely related discipline is required. In addition, applicants must exhibit a strong research potential and a commitment to teaching excellence. Qualified women and men in all areas will be considered; however, particular attention will be paid to applicants with a strong interest in computer architecture, operating systems, compiler design, parallel processing, graphics, or software engineering.

This position reflects the continuing commitment to growth in the computer science department. Currently, the department has fifteen full time faculty, and offers a challenging graduate program leading to an M.S. and a Ph.D. The department is especially strong in the areas of artificial intelligence and software engineering, and its faculty are receiving funded support for research in these areas from a number of local and national sources. Teaching resources in the department includes Harris HCX-9 minicomputer, a number of networked SUN workstations, two Symbolics machines, and networked personal computers. In addition, the F.I.T. computing center provides access to DEC mainframes, minicomputers and VAX stations.

The Florida Institute of Technology is a private institution located in central Florida on the Atlantic coast. Its total enrollment is around 8,000 F.I.T.'s location on the Space Coast is well suited for research collaboration with area industry and government, including NASA-Kennedy Space Center and its major contractors, Harris Corporation, and a number of smaller "high tech" companies. The Melbourne area is a lovely, relatively undiscovered, haven for sun and surf worshipers.

Interested applicants should send a current resume and names of three references to: Dr. Dan Tamir, Recruitment Chair, Department of Computer Science, Florida Institute of Technology, 150 W. University Blvd., Melbourne, FL 32901. Email: tamir@cs.fit.edu.

F.I.T. is an equal opportunity employer. Applications from women, ethnic minorities, and the handicapped are especially welcomed.

**HAWAII PACIFIC UNIVERSITY**

Hawaii Pacific University has openings for one or more Computer Science career faculty, Assistant or Associate Professor rank, commencing August 24, 1991. Appropriate master's degree, and teaching or professional experience, are minimum qualifications; doctorate preferred. Send c.v., list of five references, and transcripts postmarked no later than April 1, 1991 to: Dr. Arnold Lipkind, Hawaii Pacific University, 1188 Fort Street, #446, Honolulu, Hawaii 96813. Equal Opportunity/Affirmative Action Employer.

**NORTHERN ARIZONA UNIVERSITY**  
Computer Science and Engineering

Northern Arizona University, College of Engineering and Technology is seeking applicants for a tenure track assistant professor position beginning Fall 1991. Applicant must have a Ph.D. in computer or electrical engineering with expertise in digital design, computer architecture, real time systems and microprocessor applications. Industrial experience/teaching desirable. Position will remain open until filled. Applications will be reviewed as they are received. Direct inquiries and applications to Lanny Mullens, Chair, Department of Computer Science and Engineering, College of Engineering and Technology, Northern Arizona University, Box 15600, Flagstaff, AZ 86011-1560. Northern Arizona University is a committed Equal Opportunity Affirmative Action Institution. Minorities, Veterans, Women and Handicapped are encouraged to apply.

**INDIANA-PURDUE UNIVERSITY  
AT FORT WAYNE**  
Department of Computer Science

Applications are invited for tenure-track positions in Information Systems and Computer Science. For the MIS position a Ph.D. or equivalent in Computer Science, MIS, or a related discipline is required. For the Computer Science position, a Ph.D. or equivalent in Computer Science or related discipline is desired; a Master's degree is required. Duties will center on teaching with scholarly activity and professional growth expected. Salaries are competitive, and the fringe benefit package is excellent. Rank and salary will be commensurate with experience.

Send vita including the names of three professional references to Dr. James L. Silver, Chair, Department of Computer Science, IPFW, Fort Wayne, IN 46805-1499. IPFW is an Affirmative Action/Equal Opportunity Employer.

**EXECUTIVE POSITION**



Carnegie Mellon University  
Software Engineering Institute

# Technology Division Director

The Software Engineering Institute (SEI) is a federally funded research and development center (FFRDC) sponsored by the Department of Defense under contract to Carnegie Mellon University. The SEI mission is to provide leadership in advancing the practice of software engineering. We are looking for a candidate with proven management skills to fill the newly created position of **Director of the Technology Division**.

## Responsibilities

- Manage, motivate and build the division team, (70-100 technical staff) in focus areas of real-time/distributed systems, process and risk management, trusted fault tolerant systems, and software engineering methods/tools
- Improve the practice of software engineering by bringing promising approaches to the stage where they are ready for widespread use
- Participate with other division directors in developing and maintaining the SEI strategy and business plan

## Qualifications

- A demonstrated record of technical and managerial accomplishment
- Extensive experience with software engineering advanced technology
- Demonstrated leadership at the program management level or above with emphasis on motivating excellence
- PhD in computer science, electrical engineering or a related field is highly desirable

## Respond to:

Sally Miller (F-4)  
Software Engineering Institute  
Carnegie Mellon University  
Pittsburgh, PA 15213

The Software Engineering Institute is sponsored by the Department of Defense. Carnegie Mellon University is an equal opportunity/affirmative action employer. U.S. citizenship or resident alien status required.

**WRIGHT STATE UNIVERSITY**  
**Department of Computer Science**  
**and Engineering**

Applicants are invited for tenure-track and visiting faculty positions at all ranks. The successful candidate must have a Ph.D. in computer science, computer engineering, or equivalent background and have demonstrated forward looking and creative research. Further desired attributes include: capability to direct Ph.D. candidates in computer science or computer engineering and the ability to acquire funds and/or direct research projects. Preferred technical areas are distributed systems, networking, and database, but other areas will be considered. Rank and competitive salaries are determined by qualifications and experience.

The university is located in a high technology environment among industrial/military research and development facilities, including Wright Patterson Air Force Base and NCR. Department strengths include a fully networked Unix environment of Sun & DEC workstations; Cray access; graduate laboratories in AI, optical computing, neural networks, and robotics; established research programs; industrial/military support; degree programs in both computer science and computer engineering; and a large graduate student population.

Please submit a detailed resume including names of three references to: CSNET address - amcaulay@cs.wright.edu or Alastair D. McAulay, NCR Distinguished Professor and Chair, Department of Computer Science and Engineering, Wright State University, Dayton, Ohio 45435. Pending availability of funding, reviewing for positions will begin February 15, 1991 and continue monthly until positions are filled or until September 1, 1991.

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**CLARKSON UNIVERSITY**  
**Electrical and Computer Engineering**

Applications are invited for a tenure-track faculty position as Assistant/Associate/Full Professor in the area of computer engineering. Responsibilities include undergraduate and graduate teaching and development of a research program. A doctorate is required. Review of applications will begin on March 31st and will continue until the position is filled.

The department offers programs at the B.S., M.S., and Ph.D. levels. Last year 196 bachelors, 15 masters, and 7 doctorates were awarded, and research funding reached more than one million dollars. Principle research areas include distributed and parallel computation, artificial intelligence, image and signal processing, neural networks, robotics and control, communication systems, solid state devices, electromagnetic scattering, power systems, and electromagnetic devices. There are research labs in artificial intelligence and neural computing, VLSI design, robotics, lasers and optics, solid state device fabrication, high voltage engineering, and dielectric breakdown.

Clarkson is an independent university specializing in engineering, science and management with an enrollment of 3300

students, including 400 graduate students. Located in northern New York, Clarkson is midway between the Adirondack Mountains and the St. Lawrence River, 80 miles from Lake Placid and a two-hour drive from Ottawa and Montreal. Send applications to Professor Henry Domingos, Chairman, Department of Electrical and Computer Engineering, Clarkson University, Potsdam, New York 13699-5720. Clarkson is an Equal Opportunity/Affirmative Action Employer. Position No. 245.

**THE UNIVERSITY OF TENNESSEE**  
**AT CHATTANOOGA**

Tenure track position in Computer Science at the rank of Assistant Professor. Applicants must have a Ph.D. in Computer Science or a related field. Applicants with experience and/or training in Software Engineering are especially encouraged but those with interests in other areas are also welcome.

UTC offers B.S. and M.S. degrees in Computer Science. It is the site of Tennessee's Center of Excellence for Computer Applications. Available resources include IBM 3090 and 4381 systems, an HP950, several Unix-based workstations and numerous microcomputers.

Chattanooga, located in one of the country's most scenic areas, offers excellent recreational opportunities and a cost of living below the national average. Send applications to:

Dr. Jack Thompson, Head  
Computer Science Department  
School of Engineering  
University of Tennessee at Chattanooga  
615 McCallie Avenue  
Chattanooga, TN 37403  
Phone (615) 755-4349

Bit Net Address is: cjt@utcm

Applications will be reviewed beginning February 1, 1991. An appointment will be made as soon as the successful candidate is selected.

The University of Tennessee at Chattanooga is an equal employment opportunity/affirmative action/Title IX/Section 504 institution.

**THE UNIVERSITY OF AKRON**  
**Head-Department of**  
**Mathematical Sciences**

The Department of Mathematical Sciences invites applications and nominations for the position of department head. A Ph.D. in the mathematical sciences (mathematics, applied mathematics, statistics, or computer science) and a strong commitment to teaching and research are required. Some administrative and/or professional experience in a mathematical sciences Ph.D. program is desirable. The Department consists of thirty-seven full-time faculty members and offers BS degrees in mathematics, applied mathematics, statistics, and computer science, and MS degrees in mathematics, applied mathematics, and statistics. The department has proposed graduate programs for the MS in Computer Science, and the Ph.D. in Applied Mathematics.

The University of Akron is the third largest state university in Ohio (30,000 day and evening students) and offers a multitude of associate, bachelors, masters, and doctorate degree programs in the physical and social sciences, engineering, and education.

Review of applications will begin April 15, 1991 and continue until the position is filled. Tentative inquiries are desirable and will be treated confidentially. Please send a curriculum vita and names of at least three references to: Dr. Chand Midha, Chair, Search Committee, Department of Mathematical Sciences, The University of Akron, Akron, OH 44325-4002. The University of Akron is an equal opportunity/affirmative action employer. Women and minorities are encouraged to apply.

**WEST VIRGINIA UNIVERSITY**  
**EXTENSION SERVICE**  
**Research Assistant Professor for**  
**Systems Administration**

WVU/ES seeks applicants for a Research Assistant Professor for Systems Administration, a non-tenured position to be continued on an annual basis, having principal technical responsibility for computer and communication systems within the organization and with external systems for special projects. Incumbent will work as a team member with co-workers and clients, assess requirements, prepare and implement plans and evaluations, and secure and maintain external project funding.

Ph.D. and MS+ in Computer Science, Electrical Engineering, or related, and minimum five years' post-BS work experience, in systems including VM, VMS, AOS/VS, OS/400, System V, AIX, Ultrix, OS/2, and DOS; languages including C/Shell, Pascal, and SAS; analog and digital communications including TCP/IP, Token Ring, Ethernet, wire, fiber, and microwave; and CNC and CIM. Salary is commensurate with professional qualifications.

Submit letter, resume, and 3 references to John T. Grasso, Search Chair, WVU Extension Service, 415 Knapp Hall, Morgantown WV 26506-6031; or write or call 304-293-2431 for additional information. WVU/ES is an EO/AA employer.

**UNIVERSITY OF WISCONSIN-**  
**MADISON**  
**Faculty Position**

The Department of Electrical and Computer Engineering invites applications for a possible tenure or tenure-track position. A Ph.D. degree is required, and successful candidates are expected to participate in both teaching and research activities. Applicants in all areas of computer engineering are invited to apply. Rank and salary will be commensurate with qualifications and experience. Send resume and names of three references to Bahaa E.A. Saleh, Chairman, Department of Electrical and Computer Engineering, University of Wisconsin-Madison, 1415 Johnson Drive, Madison, WI 53706, an equal opportunity/affirmative action employer.



# BOOK REVIEWS

Editor: Guy Johnson, Department of Information Technology, Rochester Institute of Technology, 1 Lomb Memorial Drive, Rochester, NY 14623

## *Parallel Logic Programming Techniques*

Stephen Taylor (Prentice Hall, Englewood Cliffs, N.J., 1989, 205 pp., \$39.00)

Although this book identifies the author's affiliation with the California Institute of Technology, it does not provide any biographical information; however, it is clear that the book's technical content reveals recent research conducted at the post-doctoral level. In fact, Taylor makes several references to "this thesis" when discussing technical issues.

The author's concept is to "construct parallel applications by recursively specifying process structures." Based on this, he describes experimental techniques for developing, compiling, and optimizing parallel applications using flat concurrent-logic programming languages as the basis for design and implementation.

The subject material begins with a general discussion of methods used to program different parallel architectures and introduces Flat Concurrent Prolog (FCP), an object-oriented concurrent-logic paradigm based on asynchronous communication. From this foundation, Taylor continues with a discussion of FCP implementation techniques, parallel algorithms, a compilation strategy based on decision graphs (an abstract program representation), and optimization techniques for improving the performance of various high-level communication protocols. Taylor demonstrates how these techniques, algorithms, and decision graphs can be represented as abstract machine instructions. Parallel interpretation of these instructions is then performed by an abstract machine emulator incorporated into the runtime environment of an Intel hypercube.

The book is well written with a good top-down organization, which Taylor robustly documents up front, where it best serves the reader. The subject material is broad in scope, yet Taylor does a superb job of focusing the discussion by refer-

encing the literature (158 references). In this manner, he has eliminated a re-hash of well-publicized ideas and concentrated on describing "what is new."

Although there are instances within the text where a more thorough discussion would have been appropriate, I found that the book was generally self-contained — for example, in Chapter 3, where Taylor uses FCP language semantics to establish the background for the reader to understand the syntax of the remaining chapters. Unfortunately, Taylor defers discussion of the semantics to the referenced literature. For me, this resulted in a reading pause accompanied by a dislocated train of thought.

Additionally, the brevity of Taylor's definitions for unification, reduction, success, failure, and suspension required me to jump ahead to Chapters 4 and 5 to gain a better understanding of these very important concepts. Taylor says, "Understanding logic programming is largely a matter of gaining an appreciation of [unification] and a small number of programming techniques which employ it." A smoother description of the unification/reduction process would enable the reader to quickly transition from an elementary to a detailed understanding of the subjects. However, once past this slight perturbation, you can sense where Taylor's going and what techniques he's employing to get there. In fact, the intensity of my reading reached peak level prior to Chapter 5 and held there for the remainder of the book.

The book describes typical problems encountered in parallel programming, such as computational deadlock, data starvation, dynamic-processor load balancing, synchronization of processor communication, and how concurrent logic-programming techniques can be em-

ployed to solve these problems. Realizing that the single most difficult problem in parallel processing today is finding a method for making parallel programming easier, I believe Taylor has made a valuable contribution toward this goal. I thoroughly enjoyed reading the book and discovered that it sparked my imagination with the vision of how Taylor's work can be applied to the development of a truly portable parallel-programming language.

Overall, the book's technical content is comprehensive and well structured; however, the subject material is best treated at the advanced-graduate level, where the student might be instructed to implement dynamic-load balancing, process mapping, and code-mapping tools for a virtual machine (for example, a re-configurable multicomputer architecture), as described in Chapter 8. The book will serve as a valuable reference for the professional engineer or computer scientist who is conducting parallel-processing research. Additionally, I recommend it to anyone interested in parallel programming, logic programming, and computer science in general.

As eloquently stated in the book's foreword by Ehud Shapiro of the Weizmann Institute of Science,

The book offers a model of how such an investigation [efficiently mapping an abstract computational model into concrete parallel computer architectures, either existing or envisioned] can be conducted, and poses a challenge in depth, scope, and performance results to other approaches attempting to bridge the gap between the human programmer and the concurrent computer.

Dana B. Harris  
Presearch Inc.  
Syracuse, N.Y.

## *Database Design and Implementation*

Leszek A. Maciaszek (Prentice Hall, Englewood Cliffs, N.J., 1990, 382 pp., \$41.00)

There are numerous books on the market on database management and theory, as well as on different aspects of system analysis. This one is probably the first that provides a practical, down-to-earth methodology for the entire life cycle of

database development and use. The book's most important feature is its presentation of an integrated treatment of database design from conception to maintenance of the final product. It is full of practical information on how to

handle numerous technical problems that arise in designing a database from scratch.

The reader is systematically taken through different database design phases: requirement analysis, conceptual struc-

ture design, logical and physical schema, user applications, and maintenance and upgrade. The chapter on requirement analysis is particularly interesting; many important concepts are carefully introduced, such as strategic planning, cost-benefit analysis, time estimation, and dataflow modeling. The author gives examples of how these concepts transition to the next phase of design, namely, the conceptual structure.

The treatment of conceptualization mainly uses Peter Chen's entity-relationship model, suitably enhanced to provide adequate semantic support. Logical schema design is treated within the relational model framework. Topics such as conversion of primitive entity-relationship constructs to different (univocal, singular, and nonunivocal) unary, binary, and ternary relationships, as well as to generic and aggregate relationships, are treated in precise detail. When discussing physical schema, the author explained placement strategies, index compression, B-tree structures, storage estimates (including good examples from dBase II and Oracle), and the effectiveness of an internal model in physical design. The last two chapters deal with user applica-

tions (mostly structured query language oriented) and maintenance issues.

The book has many strengths. It does not focus on database theory, but rather on how to use the theory. Throughout the chapters, the author emphasizes how to solve a specific problem from a practical viewpoint at each stage of database design. Anybody who is interested in designing a database would immensely benefit from reading this book. Two useful features are a rich set of references and a section on further reading at the end of each chapter. The reference lists are up-to-date and reasonably exhaustive, and the sections on further reading go a long way toward helping readers extract additional pertinent information.

Many people will find the book very useful, including practicing database engineers (administrators, application programmers, and system analysts), as well as researchers and students who are interested in seeing a global picture of the database design process. Although there is a brief chapter on design theory, the author assumes that the reader is familiar with basic database design and high-level language programming. To quote Maciaszek,

A reader who suspects that immediate study of the book might be tough going is advised to first read one of the introductory texts on databases, such as *An Introduction to Database Systems* by C. J. Date (Addison-Wesley, 4th ed., 1986).

Also, some knowledge of interactive structured query language would certainly help the reader to understand some subtleties in the examples. The book may be used as a primary or companion text for a graduate course in databases, information systems, or systems analysis.

I'd hesitate to recommend this text for independent study or undergraduate courses for one important reason: None of the chapters has a problem set. In my opinion, a good textbook or independent study book must contain well-designed exercise problems. But then, this is about the only drawback that comes to mind while reading the book. As a reference guide for anybody interested in database design, the book will stand out. I did enjoy reading it.

Pradip K. Srimani  
Colorado State University

## Naturally Intelligent Systems

Maureen Caudill and Charles Butler (MIT Press, Cambridge, Mass., 1990, 304 pp., \$19.95)

This book, which starts with a wrong title and ends without a bibliography, leaves the reader a little disappointed. A better title would have been "Two Introductions to Neutral Networks."

The first introduction (the first 167 pages) is subelementary, fuzzy, and vague; the second one (the next 100 pages) is much better, but still a little imprecise.

Artificial neural networks are information processing systems (usually software, but sometimes hardware, too) that try to emulate biological neural networks (the brain). On the positive side, it would be wonderful to have an artificial brain do everything we want, but, on the negative side, we don't even know how the brain works. Even if we did know (which many consider impossible because the brain may not be cognizable), history shows that we have not emulated nature in many of our other activities — for example, in transportation, construction, or entertainment. However, this does not mean that we shouldn't try.

The issue is realism: to see what reasonably can be done and what can not. It seems that this is the most difficult problem in artificial neural networks. Some scientists try to emulate the brain no matter what; others are more flexible and

ready to compromise. The latter ones seem to have a better future.

The book's first introduction vaguely describes several characteristics of artificial neural networks. The authors compare them with biological neural networks, try to explain several memory types (for example, associative, distributed, crossbar associative, adaptive, and competitive filter associative), and give some ideas about learning methods such as observational, Hebbian, Grossberg, differential, autonomous, instrumental, and classical conditioning).

The crossbar associative memories are presented using the energy surface and matrix representations. Adaline, Madaline, and polynomial Adaline (called Padaline) are featured as examples of adaptive filter associative memories. The training techniques — graded, supervised, and unsupervised — are briefly presented.

The style of this first introduction can be illustrated with a quote it makes at one juncture: "One feature of parabolas is that they have a bottom." This naive approach is inappropriate for such a complex and mathematical topic as neural networks.

The second introduction better covers more advanced neural networks (such as

hierarchical, back propagation, hybrid, counterpropagation, and adaptive resonance), the implementation of neural networks (including software simulation, special-purpose digital computers, and electronic or optical neural networks), and some network applications (for example, expert systems, process control, robotics, and signal processing). This second introduction concludes with a look ahead to future research.

Throughout the book, there are brief digressions into related subjects, which are displayed in shaded areas. A few are interesting (for example, Neocognitron and Net Talk), but many others are not.

The glossary contains a plethora of terms, but many definitions are imprecise, incomplete, and sometimes wrong.

The field of artificial neural networks is an advanced one and requires an appropriate level of presentation, including a good dose of rigor, clarity, and depth. This is not the case here, especially in the first introduction. Without precise definitions and a significant mathematical foundation, the talk about artificial neural networks remains just that — and not very useful talk at that.

Michael M. Dediu  
Dediu Computer Consultants

# THE OPEN CHANNEL

"Any clod can have the facts, but having opinions is an art."

Charles McCabe, San Francisco Chronicle

Will Tracz, IBM, Federal Sector Division, Mail Drop 0210, Owego, NY 13827  
E-mail [tracz@0wgvm0.iinus1.ibm.com](mailto:tracz@0wgvm0.iinus1.ibm.com)

## Reopening the channel

Greetings, and welcome to the Open Channel, I mean Open Channel. As your friendly Open Channel editor (alias your friendly used-program salesman), I'm extending you an open invitation to share a bit (or even a byte, if you like) of wit, wisdom, or biased opinion with other readers.

My eyes and ears are open. Being open and nonbiased, I will accept submissions from anybody (as I have no standards to lower).

The sky is the limit on ideas for reopening the channel, but 1,000 words is the limit on length. I am open to topic suggestions, and I welcome any cynical, sarcastic, pragmatic or dogmatic observations, revelations, or hallucinations you might want to share.

While I can assure you that the submissions for this column don't need to include the word "open" in every sentence, I am reasonably optimistic that they'll provide the

reader, as well as the contributor, with a valuable outlet for coping with our profession's everyday trials and tribulations.

Will Tracz  
Open Channel Editor

*Computer's Open Channel department was created by Computer Society member James H. Haynes and edited by him for many years. In the February 1975 issue, the then-called "Haynes' Cookbook" became "Open Channel."*

*Our new editor, Will Tracz, has contributed many items in previous issues as the "used-program salesman." His first submission was in April 1983.*

*May 1990 was the last time the department ran. It will be featured on the back page beginning this month. — Ed.*

## On the limitations of group communication

A.M. Baldassarre, University of Houston

Among mankind's universal problems, communication mediocrity stands out. Throughout history, man has attempted to create expressive means of communication — for instance, verbal languages and motion pictures — to transmit common ideas. However, no symbolic system has so far been able to express the mind's idealistic power. Even formal mathematics — which some people think of as a universal technical language — seems hopelessly inept in human intercommunication.

Although they're not the ultimate achievement in transmitting ideas, formal mathematics and VLSAL (very large scale application of logic) seem to be the most expressive means for transporting technical knowledge from one person to another. Because of this, it is extremely unlikely that teamwork would achieve very high performance — an artistic or scientific masterpiece.

Creation, or the seed for it, frequently comes as a lightning bolt of cognition. This original creative seed is a whole entity in a single mind. Because of communication limitations, it cannot be decomposed, transmitted to, and assimilated by someone else.

Let's illustrate this with some trivial geometric concepts. Suppose our ancestors had primitive ideas that could be modeled in a three-dimensional space (not my personal opinion). Idea transmission would take at least three isometric projections, if an idealistic two-dimensional communication means were available. The message receiver's task would be to reconstruct the sender's original idea and figure it out without ambiguity — spending a great deal of effort in the process.

Now let's return to the present, where contemporary man processes much more complex ideas. Modeling modern ideas should logically take much larger multidimensional proportions than modeling primitive ones. We will naively presume that these ideas are geometrically representable in 1,000-dimension space, on the average. Someone willing to communicate his or her idea should decompose it into several projections that could pass through the available channel. However, no known transmission method could support even one-tenth of such spatial complexity; therefore, hundreds of projections would have to be sent.

A receiver who is willing to reconstitute the original information would hereafter have to deal with hundreds of meaningless projections. The global meaning of the sender's idea would clearly be lost in the transmission process, because of the projective decomposition ambiguity applied to the original idea.

Our common languages, notations, and symbols are doomed because their communication spaces are physically limited to low complexity (two dimensional). They display such enormous ambiguities (among other flaws) that no pure, global idea could possibly be transmitted as a whole without tremendous syntactic and semantic loss. A blessing for the future would be greater semantic encoding/decoding schemes for our languages (even spoken languages like English), which currently fail to sustain correct information acquisition and disclosure. As a consequence, most sciences that are strongly based on human intercommunication are in jeopardy (for example, very large software projects).

Having now reached a communication wall, are we bound to information chaos?

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